

**a-Si TFT LCD Single Chip Driver  
240RGBx320 Resolution and 16.7M color**

**Datasheet**  
***Preliminary***

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## 1. Introduction

ILI9320 is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes RAM for graphic data of 240RGBx320 dots, and power supply circuit.

The dithering image processing is implemented in ILI9320 to provide the 16 million colors display quality and the Multi-domain Vertical Alignment (MVA) wide view angle display is also supported in the ILI9320.

ILI9320 has four kinds of system interfaces which are i80-system MPU interface (8-/9-/16-/18-bit bus width), VSYNC interface (system interface + VSYNC, internal clock, DB[17:0]), serial data transfer interface (SPI) and RGB 6-/16-/18-bit interface (DOTCLK, VSYNC, HSYNC, ENABLE, DB[17:0]).

In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write function and widow address function enables to display a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to transfer display the refresh data only to minimize data transfers and power consumption.

ILI9320 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9320 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9320 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, PDA and PMP where long battery life is a major concern.

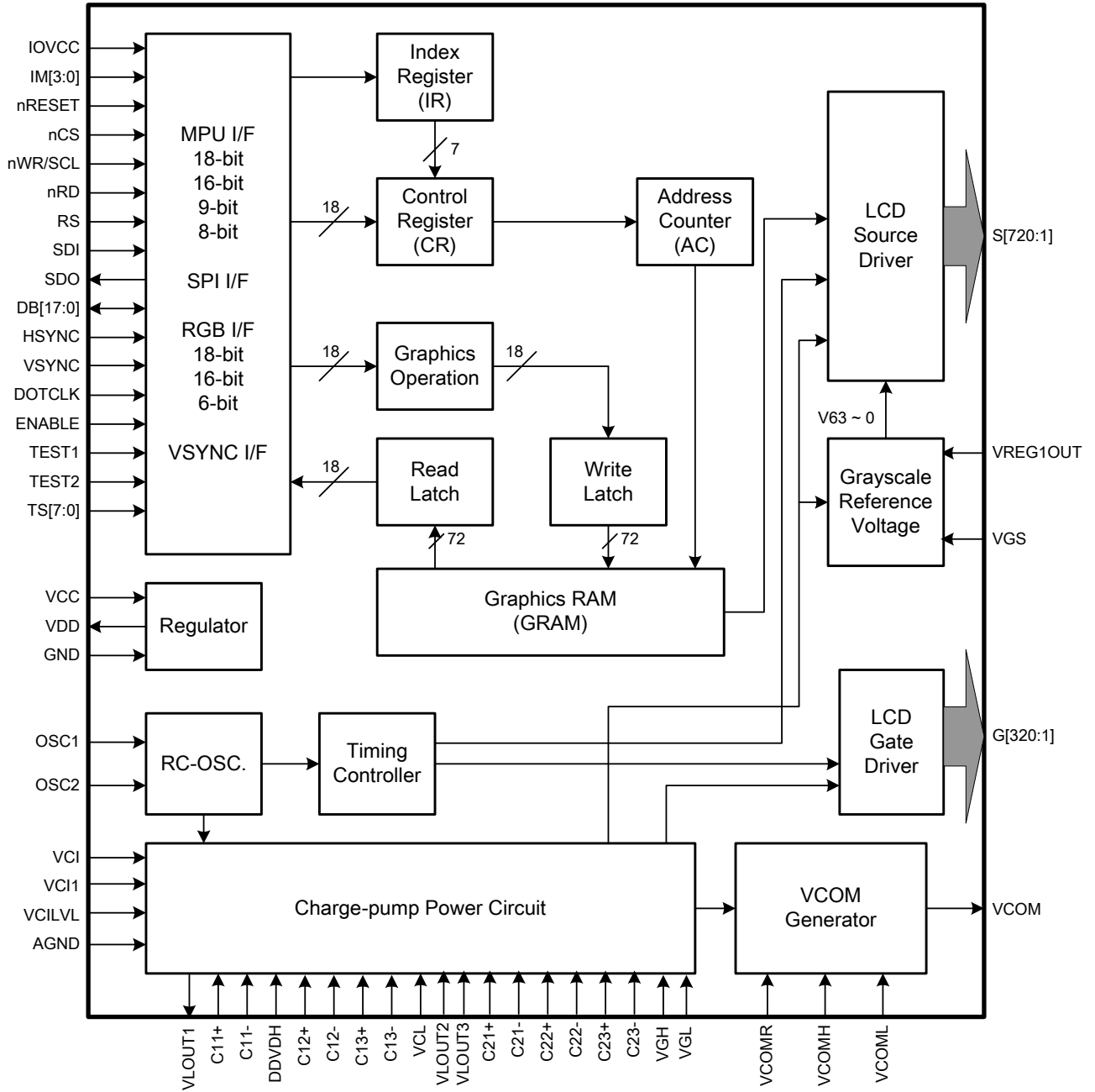
## 2. Features

- ◆ Single chip solution for a liquid crystal QVGA TFT LCD display
- ◆ 240RGBx320-dot resolution capable with real 262,144 display color
- ◆ Dithering image processing implemented to provide 16.7-million color display quality
- ◆ Support MVA (Multi-domain Vertical Alignment) wide view display
- ◆ Incorporate 720-channel source driver and 320-channel gate driver
- ◆ Internal 172,800 bytes graphic RAM
- ◆ High-speed RAM burst write function
- ◆ System interfaces
  - i80 system interface with 8-/ 9-/16-/18-bit bus width
  - Serial Peripheral Interface (SPI)
  - RGB interface with 6-/16-/18-bit bus width (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
  - VSYNC interface (System interface + VSYNC)
- ◆ n-line liquid crystal AC drive: invert polarity at an interval of arbitrarily n lines (n: 1 ~ 64)
- ◆ Internal oscillator and hardware reset
- ◆ Resizing function (×1/2, ×1/4)
- ◆ Reversible source/gate driver shift direction

- ◆ Window address function to specify a rectangular area for internal GRAM access
- ◆ Bit operation function for facilitating graphics data processing
  - Bit-unit write data mask function
  - Pixel-unit logical/conditional write function
- ◆ Abundant functions for color display control
  - $\gamma$ -correction function enabling display in 262,144 colors
  - Line-unit vertical scrolling function
- ◆ Partial drive function, enabling partially driving an LCD panel at positions specified by user
- ◆ Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- ◆ Power saving functions
  - 8-color mode
  - standby mode
  - sleep mode
- ◆ Low -power consumption architecture
  - Low operating power supplies:
    - $IOV_{cc} = 1.65V \sim 3.3V$  (interface I/O)
    - $V_{cc} = 2.4V \sim 3.3V$  (internal logic)
    - $V_{ci} = 2.5V \sim 3.3V$  (analog)
- ◆ LCD Voltage drive:
  - Source/VCOM power supply voltage
    - $DVDH - GND = 4.5V \sim 6.0$
    - $VCL - GND = -2.0V \sim -3.0V$
    - $VCI - VCL \leq 6.0V$
  - Gate driver output voltage
    - $VGH - GND = 10V \sim 20V$
    - $VGL - GND = -5V \sim -15V$
    - $VGH - VGL \leq 32V$
  - VCOM driver output voltage
    - $VCOMH = 3.0V \sim (DDVDH-0.5)V$
    - $VCOML = (VCL+0.5)V \sim 0V$
    - $VCOMH-VCOML \leq 6.0V$
- ◆ a-TFT LCD storage capacitor: Cst only



### 3. Block Diagram



## 4. Pin Descriptions

Pin Name	I/O	Type	Descriptions																																																																								
<b>Input Interface</b>																																																																											
IM3, IM2, IM1, IM0/ID	I	IOVcc	Select the MPU system interface mode																																																																								
			<table border="1"> <thead> <tr> <th>IM3</th> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>MPU-Interface Mode</th> <th>DB Pin in use</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td><b>i80-system 16-bit interface</b></td> <td><b>DB[17:10], DB[8:1]</b></td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td><b>i80-system 8-bit interface</b></td> <td><b>DB[17:10]</b></td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td><b>ID</b></td> <td><b>Serial Peripheral Interface (SPI)</b></td> <td><b>SDI, SDO</b></td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>*</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting invalid</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td><b>i80-system 18-bit interface</b></td> <td><b>DB[17:0]</b></td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td><b>i80-system 9-bit interface</b></td> <td><b>DB[17:9]</b></td> </tr> <tr> <td>1</td> <td>1</td> <td>*</td> <td>*</td> <td>Setting invalid</td> <td></td> </tr> </tbody> </table>	IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use	0	0	0	0	Setting invalid		0	0	0	1	Setting invalid		0	0	1	0	<b>i80-system 16-bit interface</b>	<b>DB[17:10], DB[8:1]</b>	0	0	1	1	<b>i80-system 8-bit interface</b>	<b>DB[17:10]</b>	0	1	0	<b>ID</b>	<b>Serial Peripheral Interface (SPI)</b>	<b>SDI, SDO</b>	0	1	1	*	Setting invalid		1	0	0	0	Setting invalid		1	0	0	1	Setting invalid		1	0	1	0	<b>i80-system 18-bit interface</b>	<b>DB[17:0]</b>	1	0	1	1	<b>i80-system 9-bit interface</b>	<b>DB[17:9]</b>	1	1	*	*	Setting invalid	
			IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use																																																																			
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When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting.																																																																											
nCS	I	MPU IOVcc	A chip select signal. Low: the ILI9320 is selected and accessible High: the ILI9320 is not selected and not accessible Fix to the DGND level when not in use.																																																																								
RS	I	MPU IOVcc	A register select signal. Low: select an index or status register High: select a control register Fix to either IOVcc or DGND level when not in use.																																																																								
nWR/SCL	I	MPU IOVcc	A write strobe signal and enables an operation to write data when the signal is low. Fix to either IOVcc or DGND level when not in use.  SPI Mode: Synchronizing clock signal in SPI mode.																																																																								
nRD	I	MPU IOVcc	A read strobe signal and enables an operation to read out data when the signal is low. Fix to either IOVcc or DGND level when not in use.																																																																								
nRESET	I	MPU IOVcc	A reset pin. Initializes the ILI9320 with a low input. Be sure to execute a power-on reset after supplying power.																																																																								
SDI	I	MPU IOVcc	SPI interface input pin. The data is latched on the rising edge of the SCL signal.																																																																								
SDO	O	MPU IOVcc	SPI interface output pin. The data is outputted on the falling edge of the SCL signal. Let SDO as floating when not used.																																																																								
DB[17:0]	I/O	MPU IOVcc	An 18-bit parallel bi-directional data bus for MPU system interface mode 8-bit I/F: DB[17:10] is used. 9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used.  18-bit parallel bi-directional data bus for RGB interface operation 6-bit RGB I/F: DB[17:12] are used. 16-bit RGB I/F: DB[17:13] and DB[11:1] are used.																																																																								

Pin Name	I/O	Type	Descriptions
			18-bit RGB I/F: DB[17:1] are used. Unused pins must be fixed either IOVcc or DGND level.
ENABLE	I	MPU IOVcc	Data ENEABLE signal for RGB interface operation. Low: Select (access enabled) High: Not select (access inhibited) The EPL bit inverts the polarity of the ENABLE signal. Fix to either IOVcc or DGND level when not in use.
DOTCLK	I	MPU IOVcc	Dot clock signal for RGB interface operation. DPL = "0": Input data on the rising edge of DOTCLK DPL = "1": Input data on the falling edge of DOTCLK Fix to the IOVcc level when not in use
VSYNC	I	MPU IOVcc	Frame synchronizing signal for RGB interface operation. VSPL = "0": Active low. VSPL = "1": Active high. Fix to the IOVcc level when not in use.
HSYNC	I	MPU IOVcc	Line synchronizing signal for RGB interface operation. HSPL = "0": Active low. HSPL = "1": Active high. Fix to the IOVcc level when not in use
FMARK	O	MPU IOVcc	Output a frame head pulse signal. The FMARK signal is used when writing RAM data in synchronization with frame. Leave the pin open when not in use.
OSC1 OSC2	I O	Oscillation resistor	Connect an external resistor for generating internal clock by internal R-C oscillation, or an external clock signal is supplied through OSC1.
<b>LCD Driving signals</b>			
S720~S1	O	LCD	Source output voltage signals applied to liquid crystal. To change the shift direction of signal outputs, use the SS bit. SS = "0", the data in the RAM address "h00000" is output from S1. SS = "1", the data in the RAM address "h00000" is output from S720. S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
G320~G1	O	LCD	Gate line output signals. VGH: the level selecting gate lines VGL: the level not selecting gate lines
VCOM	O	TFT common electrode	A supply voltage to the common electrode of TFT panel. VCOM is AC voltage alternating signal between the VCOMH and VCOML levels.
VCOMH	O	Stabilizing capacitor	The high level of VCOM AC voltage. Connect to a stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The low level of VCOM AC voltage. Adjust the VCOML level with the VDV bits. Connect to a stabilizing capacitor.
VCOMR	I	Variable resistor or open	A reference level to generate the VCOMH level either with an externally connected variable resistor or by setting the register of the ILI9320. When using a variable resistor, halt the internal VCOMH adjusting circuit by setting the register and place the resistor between VREG1OUT and AGND. When generating the VCOMH level by setting the register, leave this pin open.
VGS	I	AGND or external resistor	Reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.
<b>Charge-pump and Regulator Circuit</b>			
Vci	I	Power supply	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.3V.
AGND	I	Power	AGND for the analog side: AGND = 0V. In case of COG, connect to

Pin Name	I/O	Type	Descriptions
		supply	GND on the FPC to prevent noise.
VciLVL	I	Power supply	VciLVL must be at the same voltage level as Vci. VciLVL=2.5V ~ 3.3V. Connect to the external power supply. In COG case, connect the VciLVL with Vci on the FPC to prevent noise.
VciOUT	O	Stabilizing capacitor Vci1	An internal reference voltage generated between Vci and AGND. The amplitude between Vci and DGND is determined by the VC[2:0] bits.
Vci1	I	Stabilizing capacitor Vci1	An internal reference voltage for the step-up circuit1. The amplitude between Vci and DGND is determined by the VC[2:0] bits. Make sure to set the Vci1 voltage so that the VLOUT1, VLOUT2 and VLOUT3 voltages are set within the respective specification.
VLOUT1	O	Stabilizing capacitor, DDVDH	Output voltage from the step-up circuit 1, which is generated from Vci1. The step-up factor is set by "BT" bits. VLOUT1= 4.5 ~ 6.0V Place a stabilizing capacitor between AGND.
DDVDH	O	VLOUT1	Power supply for the source driver and Vcom drive. Connect to VLOUT1 and DDVDH = 4.5 ~ 6.0V
VLOUT2	O	Stabilizing capacitor, VGH	Output voltage from the step-up circuit 2, which is generated from Vci1 and DDVDH. The step-up factor is set by "BT" bits. VLOUT2= max.15V Place a stabilizing capacitor between AGND and a shottkey diode between Vci.
VGH	I	VLOUT2	Power supply for the gate driver, connect to VLOUT2.
VLOUT3	O	Stabilizing capacitor, VGL	Output voltage from the step-up circuit 2, which is generated from Vci1 and DDVDH. The step-up factor is set by "BT" bits. VLOUT3= max. -12.5V Place a stabilizing capacitor between AGND and a shottkey diode between Vci.
VGL	I	VLOUT3	Power supply for the gate driver, connect to VLOUT3.
VCL	O	Stabilizing capacitor, VCL	VcomL driver power supply. VCLC = 0 ~ -3.3V. Place a stabilizing capacitor between AGND
C11+, C11- C12+, C12-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.
C13+, C13- C21+, C21- C22+, C22- C23+, C23-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.
VREG1OUT	I/O	Stabilizing capacitor or power supply	Output voltage generated from the reference voltage. The voltage level is set with the VRH bits. VREG1OUT is (1) a source driver grayscale reference voltage, (2) VcomH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH - 0.5)V.
<b>Power Pads</b>			
Vcc	I	Power supply	A supply voltage to the internal logic: Vcc = 2.4~3.3V
IOVcc	I	Power supply	A supply voltage to the interface pins: IM[3:0], nRESET, nCS, nWR, nRD, RS, DB[17:0], VSYNC, HSYNC, DOTCLK, ENABLE, SCL, SDI, SDO. IOVcc = 1.65 ~ 3.3V and Vcc ≥ IOVcc. In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent noise.
VDD	O	Power	Digital core power pad.

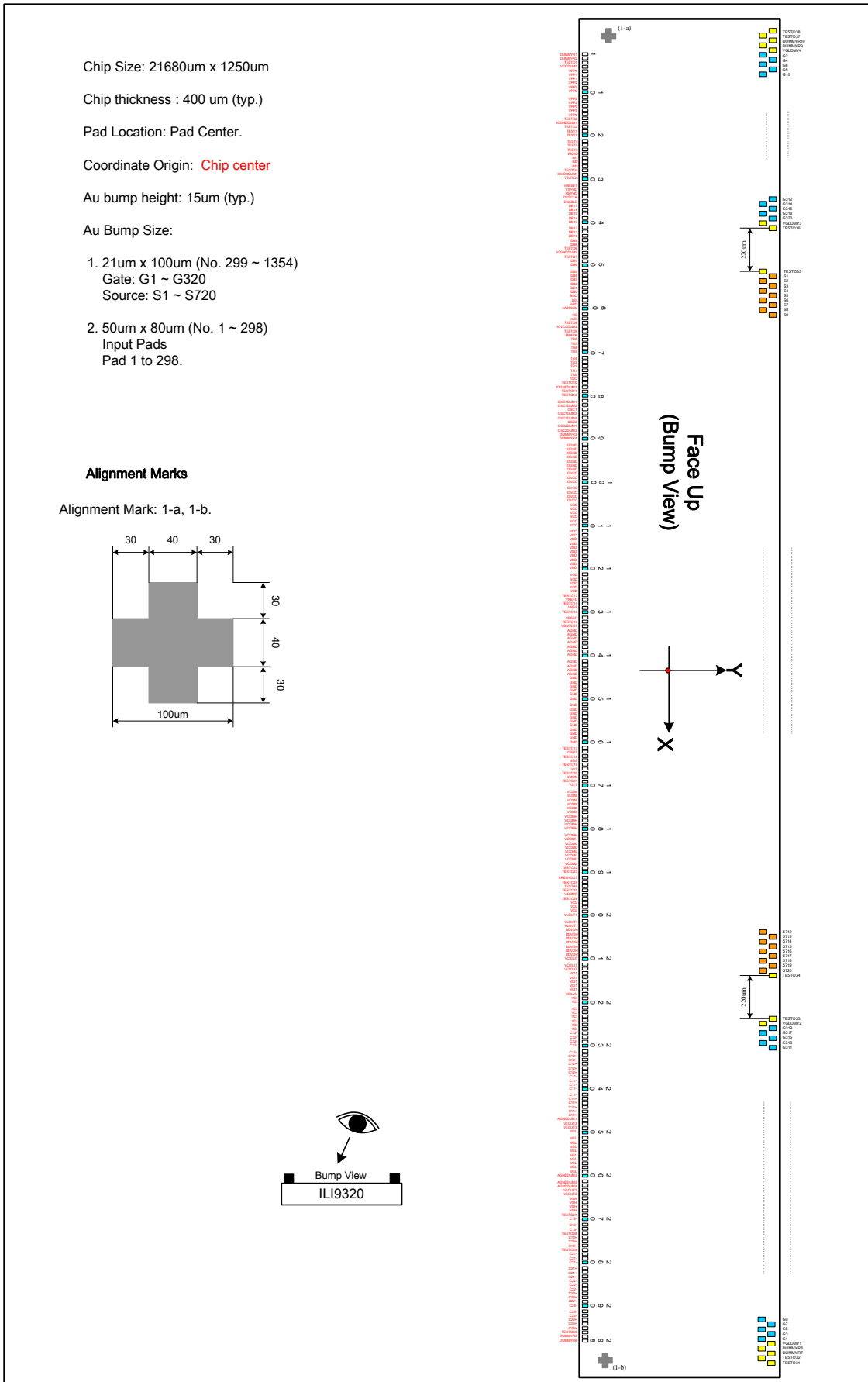
Pin Name	I/O	Type	Descriptions
			Connect them with the 1uF capacitor.
GND	I	Power supply	DGND for the logic side: DGND = 0V.
IOGND	I	Power supply	IOGND for the interface pins. IOGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
Test Pads			
V0T, V31T	-	-	Dummy pads. Connect to IOVcc, GND or leave these pins as open.
VTEST	-	-	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
VREFC	-	-	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
VREF	-	-	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
VDDTEST	-	-	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
VREFD	-	-	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
VMON	-	-	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
TESTA5	-	-	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
IOVCCDUM1~2	O	Power	Output the IOVcc voltage level. These pins are internally shorted to IOVCC
VCCDUM1	-	-	Dummy pin. Connect to IOVcc, GND or leave this pin as open.
IOGNDDUM1~3	O	Power	Output the GND voltage level. These pins are internally shorted to GND. When adjacent pins are needed to pull low, tie these pins to IOGNDDUM1~3.
OSC1DUM1~4	-	-	Dummy pads. Connect to IOVcc, GND or leave these pins as open.
OSC2DUM1~2	-	-	Dummy pads. Connect to IOVcc, GND or leave these pins as open.
AGNDDUM1	-	-	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
AGNDDUM2~4	O	Power	Output the GND voltage level. These pins are internally shorted to GND.
DUMMYR1~ 10	-	-	Dummy pads.
VGLDMY1~4	O	Open	Dummy pads. Connect to IOVcc, GND or leave these pins as open.
TESTO1~38	O	Open	Test pins. Leave them open.
TEST1, 2, 5	I	IOGND	Test pins (internal pull low). Connect to GND or leave these pins as open.
TEST3	I	IOVcc	Dummy pin. Connect to IOVcc, GND or leave these pins as open.
TEST4	I	IOVcc	Dummy pin. Connect to IOVcc, GND or leave these pins as open.
TSC	I	AGND	Dummy pin. Connect to IOVcc, GND or leave these pins as open.
TS0~8	I	OPEN	Test pins (internal pull low). Leave them open.
VPP1~3	-	Power Supply	Test pins. Must let these pads as open.

**Liquid crystal power supply specifications Table 1**

No.	Item	Description	
1	TFT Source Driver	720 pins (240 x RGB)	
2	TFT Gate Driver	320 pins	
3	TFT Display's Capacitor Structure	Cst structure only (Common VCOM)	
4	Liquid Crystal Drive Output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G320	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes VCOMH=VCOMR: Adjusted with an external resistor
5	Input Voltage	IOVcc	1.65 ~ 3.30V
		Vcc	2.40 ~ 3.30V
		Vci	2.50 ~ 3.30V
6	Liquid Crystal Drive	DDVDH	4.5V ~ 6.0V

	Voltages	VGH	10V ~ 15V
		VGL	-4.5V ~ -12.5V
		VCL	-1.9V ~ -3.0V
		VGH - VGL	Max. 30V
		Vci - VCL	Max. 6.0V
7	Internal Step-up Circuits	VLOUT1 (DDVDH)	Vci1 x2, x3
		VLOUT2 (VGH)	Vci1 x6, x7, x8
		VLOUT3 (VGL)	Vci1 x-3, x-4, x-5
		VCL	Vci1 x-1

## 5. Pad Arrangement and Coordination













No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1201	G298	-7610.0	386.5	1261	G178	-8810.0	386.5	1321	G58	-10010.0	386.5
1202	G296	-7630.0	511.5	1262	G176	-8830.0	511.5	1322	G56	-10030.0	511.5
1203	G294	-7650.0	386.5	1263	G174	-8850.0	386.5	1323	G54	-10050.0	386.5
1204	G292	-7670.0	511.5	1264	G172	-8870.0	511.5	1324	G52	-10070.0	511.5
1205	G290	-7690.0	386.5	1265	G170	-8890.0	386.5	1325	G50	-10090.0	386.5
1206	G288	-7710.0	511.5	1266	G168	-8910.0	511.5	1326	G48	-10110.0	511.5
1207	G286	-7730.0	386.5	1267	G166	-8930.0	386.5	1327	G46	-10130.0	386.5
1208	G284	-7750.0	511.5	1268	G164	-8950.0	511.5	1328	G44	-10150.0	511.5
1209	G282	-7770.0	386.5	1269	G162	-8970.0	386.5	1329	G42	-10170.0	386.5
1210	G280	-7790.0	511.5	1270	G160	-8990.0	511.5	1330	G40	-10190.0	511.5
1211	G278	-7810.0	386.5	1271	G158	-9010.0	386.5	1331	G38	-10210.0	386.5
1212	G276	-7830.0	511.5	1272	G156	-9030.0	511.5	1332	G36	-10230.0	511.5
1213	G274	-7850.0	386.5	1273	G154	-9050.0	386.5	1333	G34	-10250.0	386.5
1214	G272	-7870.0	511.5	1274	G152	-9070.0	511.5	1334	G32	-10270.0	511.5
1215	G270	-7890.0	386.5	1275	G150	-9090.0	386.5	1335	G30	-10290.0	386.5
1216	G268	-7910.0	511.5	1276	G148	-9110.0	511.5	1336	G28	-10310.0	511.5
1217	G266	-7930.0	386.5	1277	G146	-9130.0	386.5	1337	G26	-10330.0	386.5
1218	G264	-7950.0	511.5	1278	G144	-9150.0	511.5	1338	G24	-10350.0	511.5
1219	G262	-7970.0	386.5	1279	G142	-9170.0	386.5	1339	G22	-10370.0	386.5
1220	G260	-7990.0	511.5	1280	G140	-9190.0	511.5	1340	G20	-10390.0	511.5
1221	G258	-8010.0	386.5	1281	G138	-9210.0	386.5	1341	G18	-10410.0	386.5
1222	G256	-8030.0	511.5	1282	G136	-9230.0	511.5	1342	G16	-10430.0	511.5
1223	G254	-8050.0	386.5	1283	G134	-9250.0	386.5	1343	G14	-10450.0	386.5
1224	G252	-8070.0	511.5	1284	G132	-9270.0	511.5	1344	G12	-10470.0	511.5
1225	G250	-8090.0	386.5	1285	G130	-9290.0	386.5	1345	G10	-10490.0	386.5
1226	G248	-8110.0	511.5	1286	G128	-9310.0	511.5	1346	G8	-10510.0	511.5
1227	G246	-8130.0	386.5	1287	G126	-9330.0	386.5	1347	G6	-10530.0	386.5
1228	G244	-8150.0	511.5	1288	G124	-9350.0	511.5	1348	G4	-10550.0	511.5
1229	G242	-8170.0	386.5	1289	G122	-9370.0	386.5	1349	G2	-10570.0	386.5
1230	G240	-8190.0	511.5	1290	G120	-9390.0	511.5	1350	VGLDMY4	-10590.0	511.5
1231	G238	-8210.0	386.5	1291	G118	-9410.0	386.5	1351	DUMMYR9	-10610.0	386.5
1232	G236	-8230.0	511.5	1292	G116	-9430.0	511.5	1352	DUMMYR10	-10630.0	511.5
1233	G234	-8250.0	386.5	1293	G114	-9450.0	386.5	1353	TESTO37	-10650.0	386.5
1234	G232	-8270.0	511.5	1294	G112	-9470.0	511.5	1354	TESTO38	-10670.0	511.5
1235	G230	-8290.0	386.5	1295	G110	-9490.0	386.5				
1236	G228	-8310.0	511.5	1296	G108	-9510.0	511.5				
1237	G226	-8330.0	386.5	1297	G106	-9530.0	386.5				
1238	G224	-8350.0	511.5	1298	G104	-9550.0	511.5				
1239	G222	-8370.0	386.5	1299	G102	-9570.0	386.5				
1240	G220	-8390.0	511.5	1300	G100	-9590.0	511.5				
1241	G218	-8410.0	386.5	1301	G98	-9610.0	386.5				
1242	G216	-8430.0	511.5	1302	G96	-9630.0	511.5				
1243	G214	-8450.0	386.5	1303	G94	-9650.0	386.5				
1244	G212	-8470.0	511.5	1304	G92	-9670.0	511.5				
1245	G210	-8490.0	386.5	1305	G90	-9690.0	386.5				
1246	G208	-8510.0	511.5	1306	G88	-9710.0	511.5				
1247	G206	-8530.0	386.5	1307	G86	-9730.0	386.5				
1248	G204	-8550.0	511.5	1308	G84	-9750.0	511.5				
1249	G202	-8570.0	386.5	1309	G82	-9770.0	386.5				
1250	G200	-8590.0	511.5	1310	G80	-9790.0	511.5				
1251	G198	-8610.0	386.5	1311	G78	-9810.0	386.5				
1252	G196	-8630.0	511.5	1312	G76	-9830.0	511.5				
1253	G194	-8650.0	386.5	1313	G74	-9850.0	386.5				
1254	G192	-8670.0	511.5	1314	G72	-9870.0	511.5				
1255	G190	-8690.0	386.5	1315	G70	-9890.0	386.5				
1256	G188	-8710.0	511.5	1316	G68	-9910.0	511.5				
1257	G186	-8730.0	386.5	1317	G66	-9930.0	386.5				
1258	G184	-8750.0	511.5	1318	G64	-9950.0	511.5				
1259	G182	-8770.0	386.5	1319	G62	-9970.0	386.5				
1260	G180	-8790.0	511.5	1320	G60	-9990.0	511.5				
									Alignment mark	X	Y
									1-a	-10613.0	-468.0
									1-b	10613.0	-468.0

<p>S1 ~ S720 G1 ~ G320 DUMMY DUMMYR TESTO VGLDMY (No. 299 ~ 1354)</p>	<p>Unit: um</p>
<p>I/O Pads (No. 1 ~ 298)</p>	

## 6. Block Description

### MPU System Interface

ILI9320 supports three system high-speed interfaces: i80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

ILI9320 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9320 read the first data from the internal GRAM. Valid data are read out after the ILI9320 performs the second read operation.

Registers are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

<b>Registers selection by system interface (8-/9-/16-/18-bit bus width)</b>				I80
Function	RS	nWR	nRD	
Write an index to IR register	0	0	1	
Read an internal status	0	1	0	
Write to control registers or the internal GRAM by WDR register.	1	0	1	
Read from the internal GRAM by RDR register.	1	1	0	

<b>Registers selection by the SPI system interface</b>			
Function	R/W	RS	
Write an index to IR register	0	0	
Read an internal status	1	0	
Write to control registers or the internal GRAM by WDR register.	0	1	
Read from the internal GRAM by RDR register.	1	1	

### Parallel RGB Interface

ILI9320 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the "External Display Interface" section. The ILI9320 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is

selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

### **Bit Operation**

The ILI9320 supports a write data mask function for selectively writing data to the internal RAM in units of bits and a logical/compare operation to write data to the GRAM only when a condition is met as a result of comparing the data and the compare register bits. For details, see “Graphics Operation Functions”.

### **Address Counter (AC)**

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

### **Graphics RAM (GRAM)**

GRAM is graphics RAM storing bit-pattern data of 172,820 (240 x 320x 18/8) bytes with 18 bits per pixel.

### **Grayscale Voltage Generating Circuit**

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the  $\gamma$ -correction register to display in 262,144 colors. For details, see the “ $\gamma$ -Correction Register” section.

### **Timing Controller**

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

### **Oscillator (OSC)**

ILI9320 generates RC oscillation with an external oscillation resistor placed between the OSC1 and OSC2 pins. The oscillation frequency is changed according to the value of an external resistor. Adjust the oscillation frequency in accordance to the operating voltage or the frame frequency. An operating clock can be input externally. During standby mode, RC oscillation is halted to reduce power consumption. For details, see “Oscillator”.

### **LCD Driver Circuit**

The LCD driver circuit of ILI9320 consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). Display pattern data are latched when the 720<sup>th</sup> bit data are input. The latched data control

the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720 source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

### **LCD Driver Power Supply Circuit**

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.



## 7. System Interface

### 7.1. Interface Specifications

ILI9320 has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

ILI9320 also has the RGB interface and VSYNC interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB[17:0].

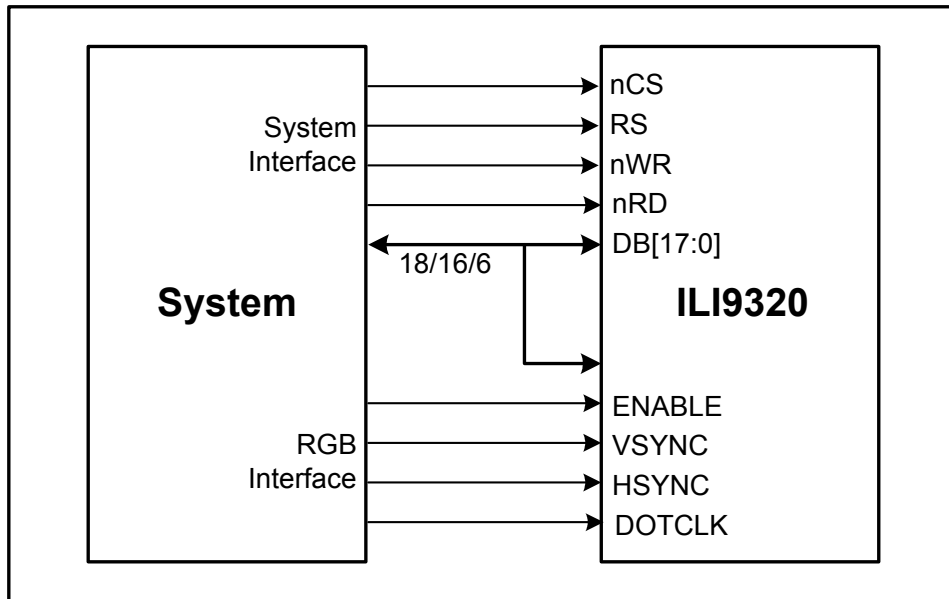
In VSYNC interface mode, the internal display timing is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface mode enables to display the moving picture display through the system interface. In this case, there are some constraints of speed and method to write data to the internal RAM.

ILI9320 operates in one of the following 4 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM[1:0])
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM[1:0] = 00)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 01)

Note 1) Registers are set only via the system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not available simultaneously.



**Figure1** System Interface and RGB Interface connection

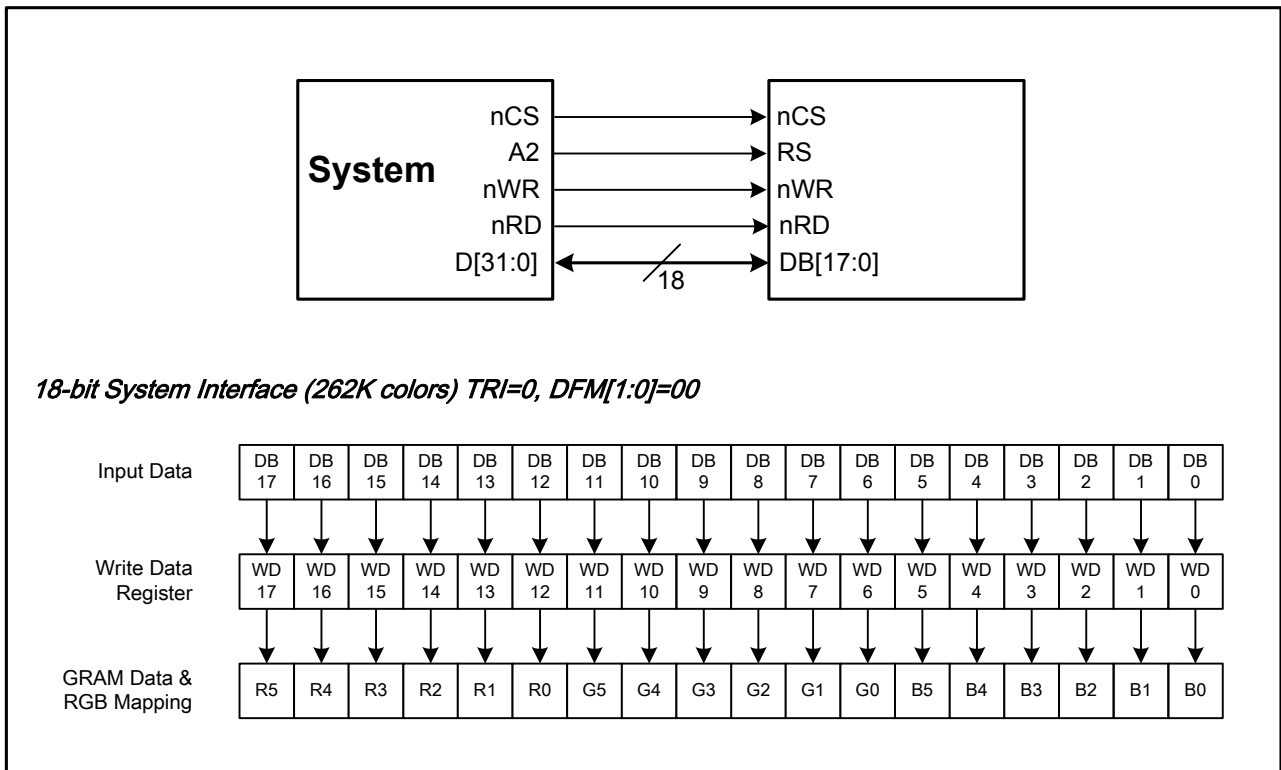
## 7.2. Input Interfaces

The following are the system interfaces available with the ILI9320. The interface is selected by setting the IM[3:0] pins. The system interface is used for setting registers and GRAM access.

IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	0	Setting invalid	
0	0	0	1	Setting invalid	
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO (DB[1:0])
0	1	1	*	Setting invalid	
1	0	0	0	Setting invalid	
1	0	0	1	Setting invalid	
1	0	1	0	i80-system 18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]
1	1	*	*	Setting invalid	

### 7.2.1. i80/18-bit System Interface

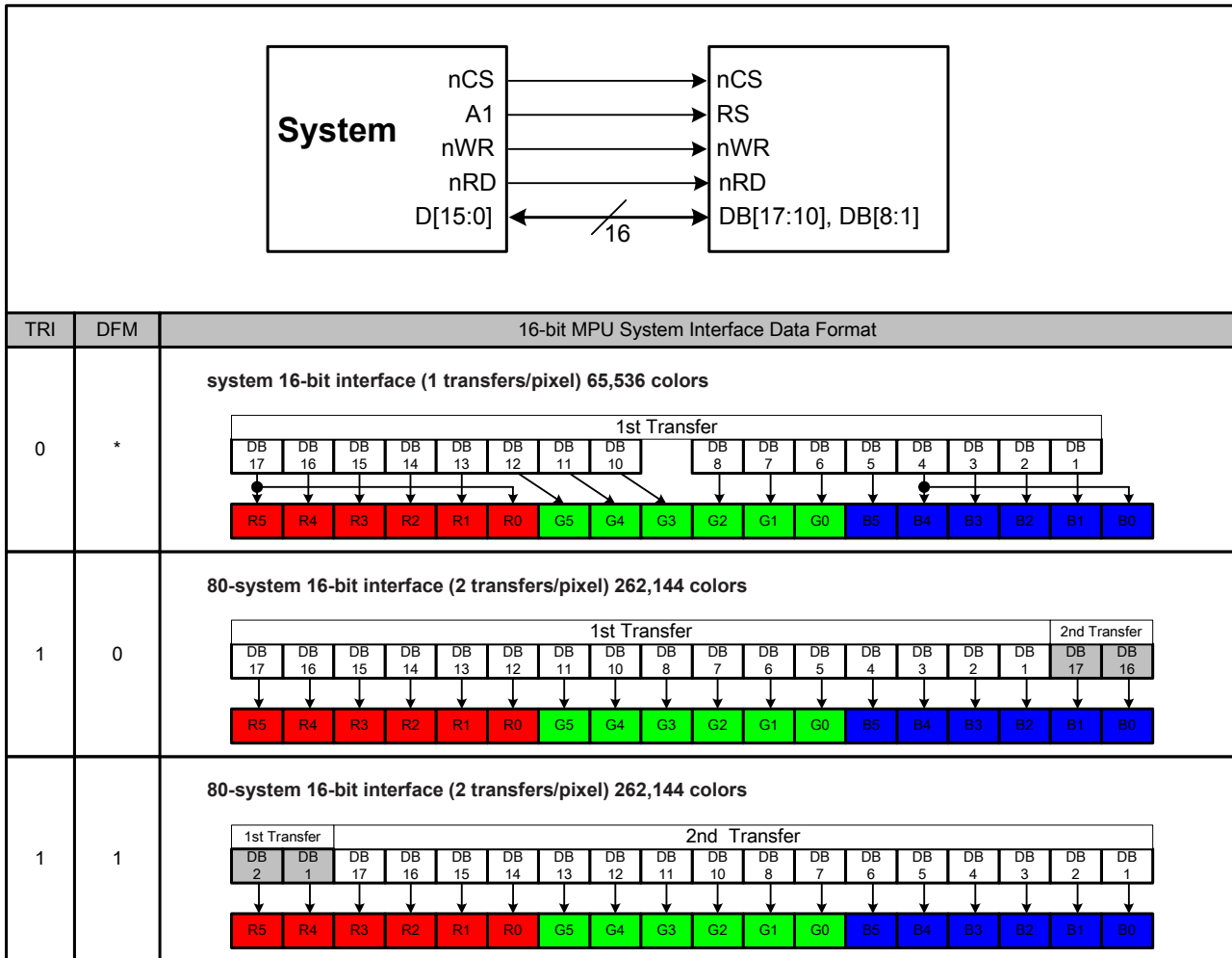
The i80/18-bit system interface is selected by setting the IM[3:0] as “1010” levels.



**Figure2 18-bit System Interface Data Format**

### 7.2.2. i80/16-bit System Interface

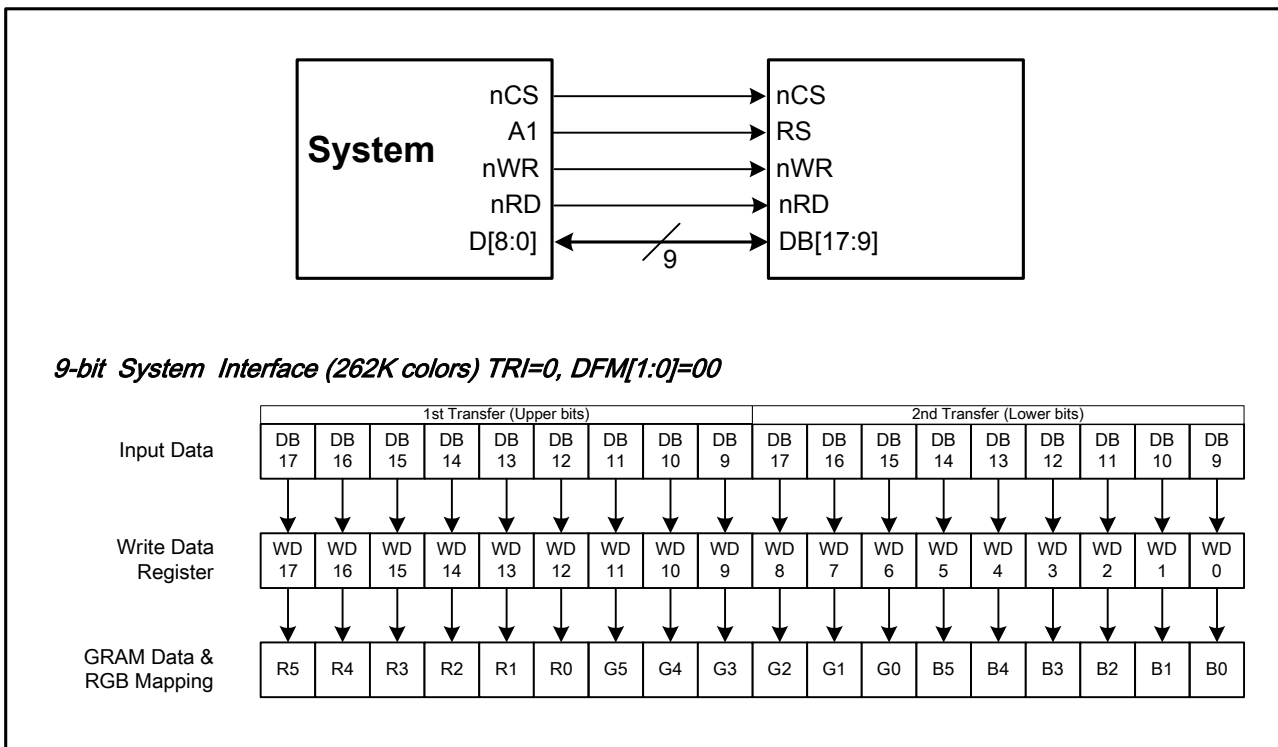
The i80/16-bit system interface is selected by setting the IM[3:0] as “0010” levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1<sup>st</sup> transfer: 2 bits, 2<sup>nd</sup> transfer: 16 bits or 1<sup>st</sup> transfer: 16 bits, 2<sup>nd</sup> transfer: 2 bits) are necessary for the 16-bit CPU interface.



**Figure3 16-bit System Interface Data Format**

### 7.2.3. i80/9-bit System Interface

The i80/9-bit system interface is selected by setting the IM[3:0] as “1011” and the DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to either Vcc or AGND.



**Figure4 9-bit System Interface Data Format**

### 7.2.4. i80/8-bit System Interface

The i80/8-bit system interface is selected by setting the IM[3:0] as “0011” and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to either Vcc or AGND.

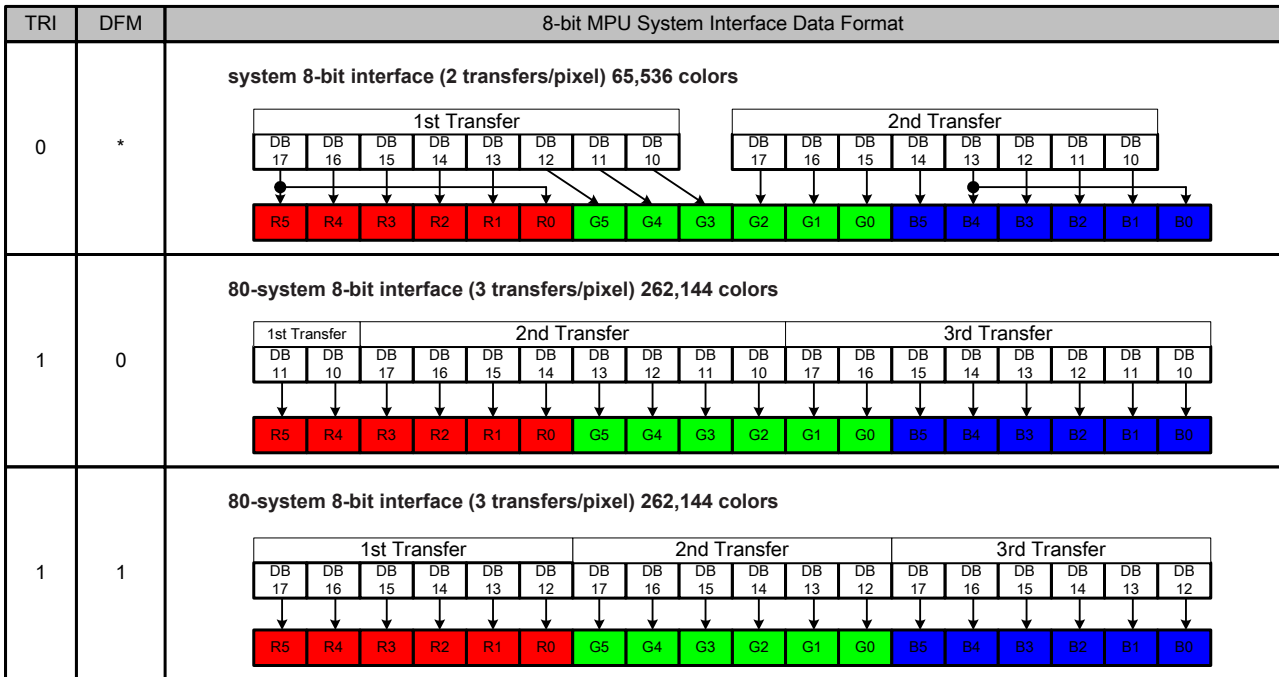


Figure5 8-bit System Interface Data Format

**Data transfer synchronization in 8/9-bit bus interface mode**

ILI9320 supports a data transfer synchronization function to reset upper and lower counters which count the transfers numbers of upper and lower byte in 8/9-bit interface mode. If a mismatch arises in the numbers of transfers between the upper and lower byte counters due to noise and so on, the “00”h register is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper byte. This synchronization function can effectively prevent display error if the upper/lower counters are periodically reset.

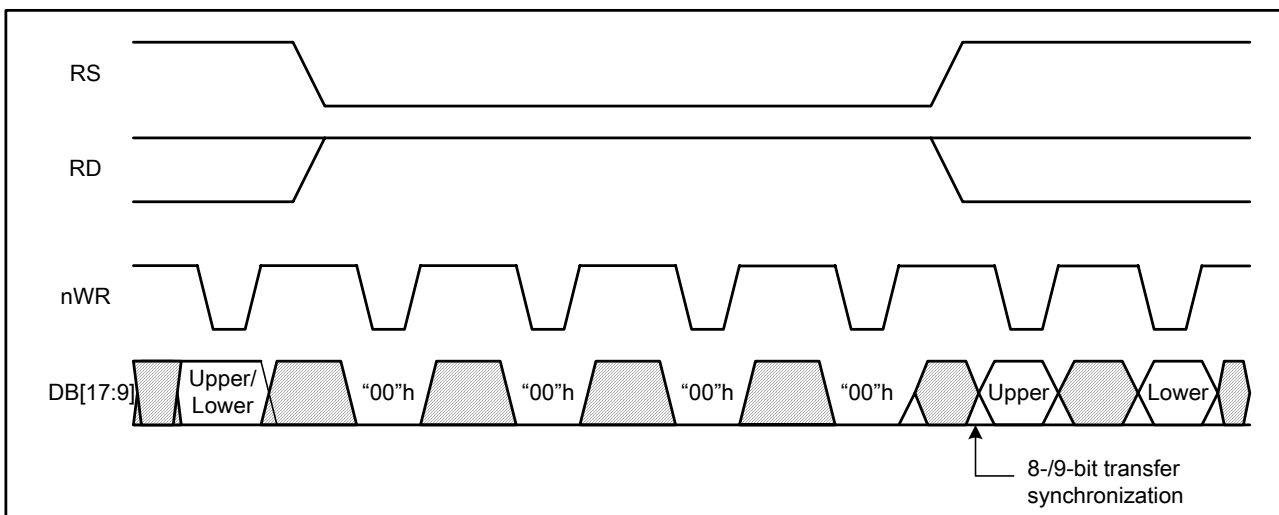


Figure6 Data Transfer Synchronization in 8/9-bit System Interface

**7.3. Serial Peripheral Interface (SPI)**

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “010x” level. The chip select pin

(nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to either IOVcc or DGND.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ILI9320.

The seventh bit of start byte is RS bit. When RS = "0", either index write operation or status read operation is executed. When RS = "1", either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is "0" and read back when the R/W bit is "1".

After receiving the start byte, ILI9320 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ILI9320 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6<sup>th</sup> byte of read back data.

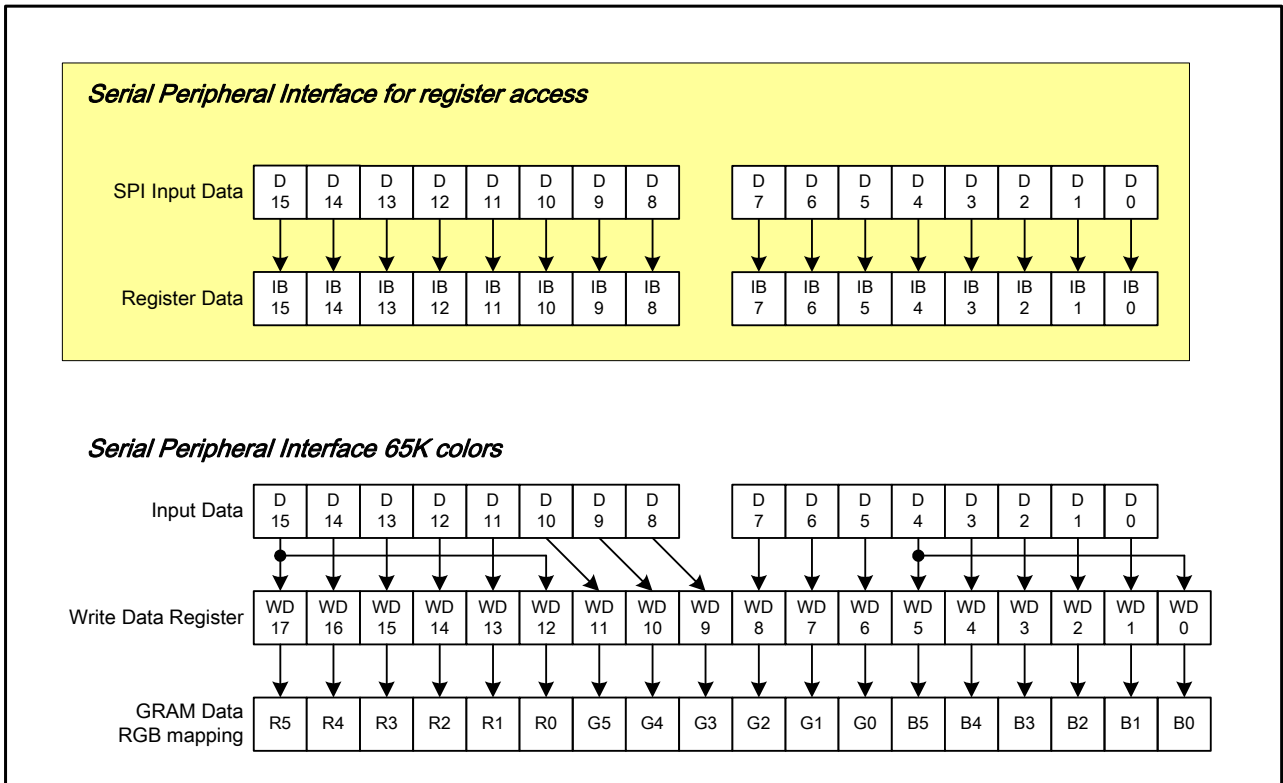
### Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8	
Start byte format	Transfer start	Device ID code					RS	R/W		
		0	1	1	1	0	ID	1/0	1/0	

Note: ID bit is selected by setting the IM0/ID pin.

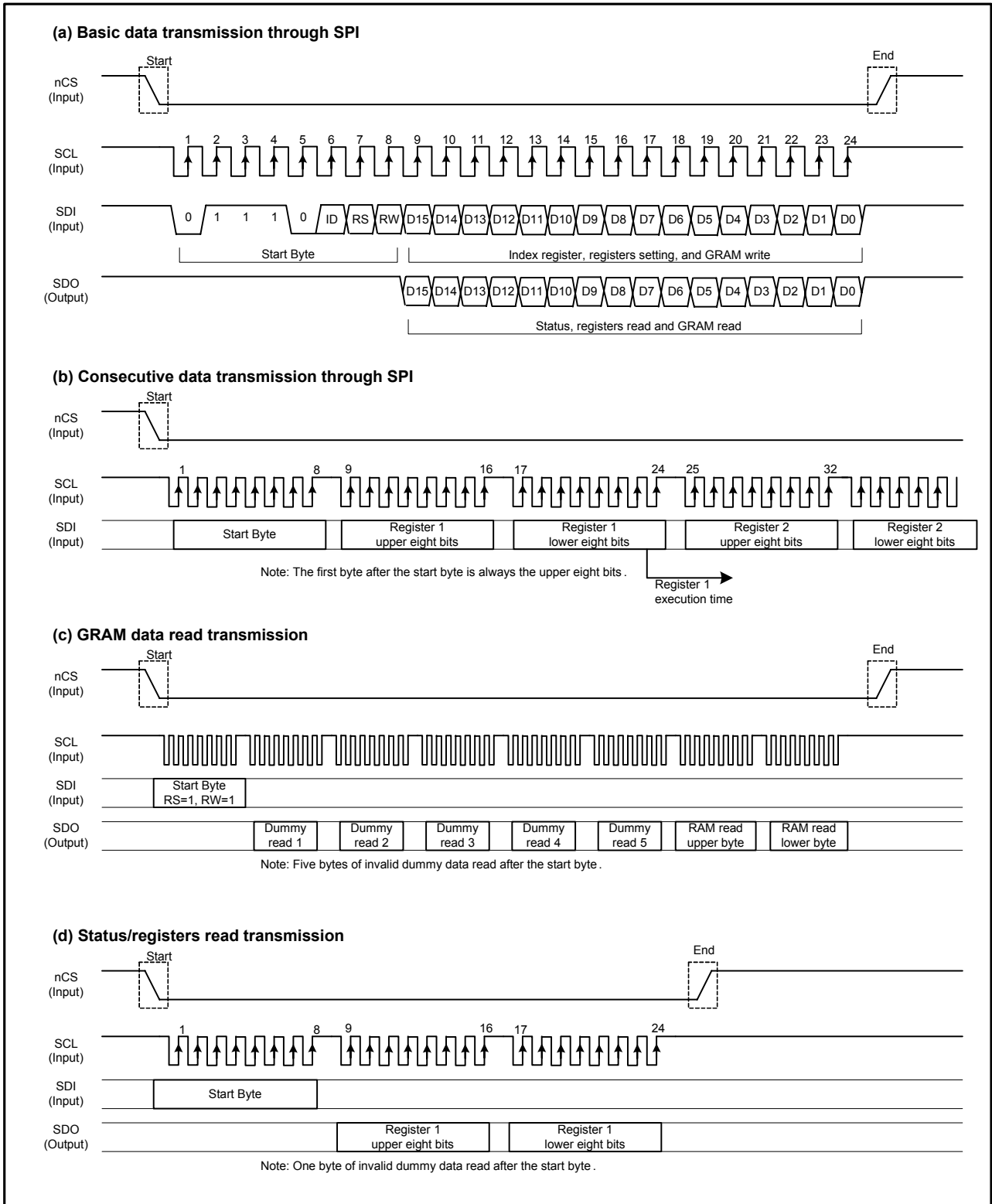
### RS and R/W Bit Function

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data

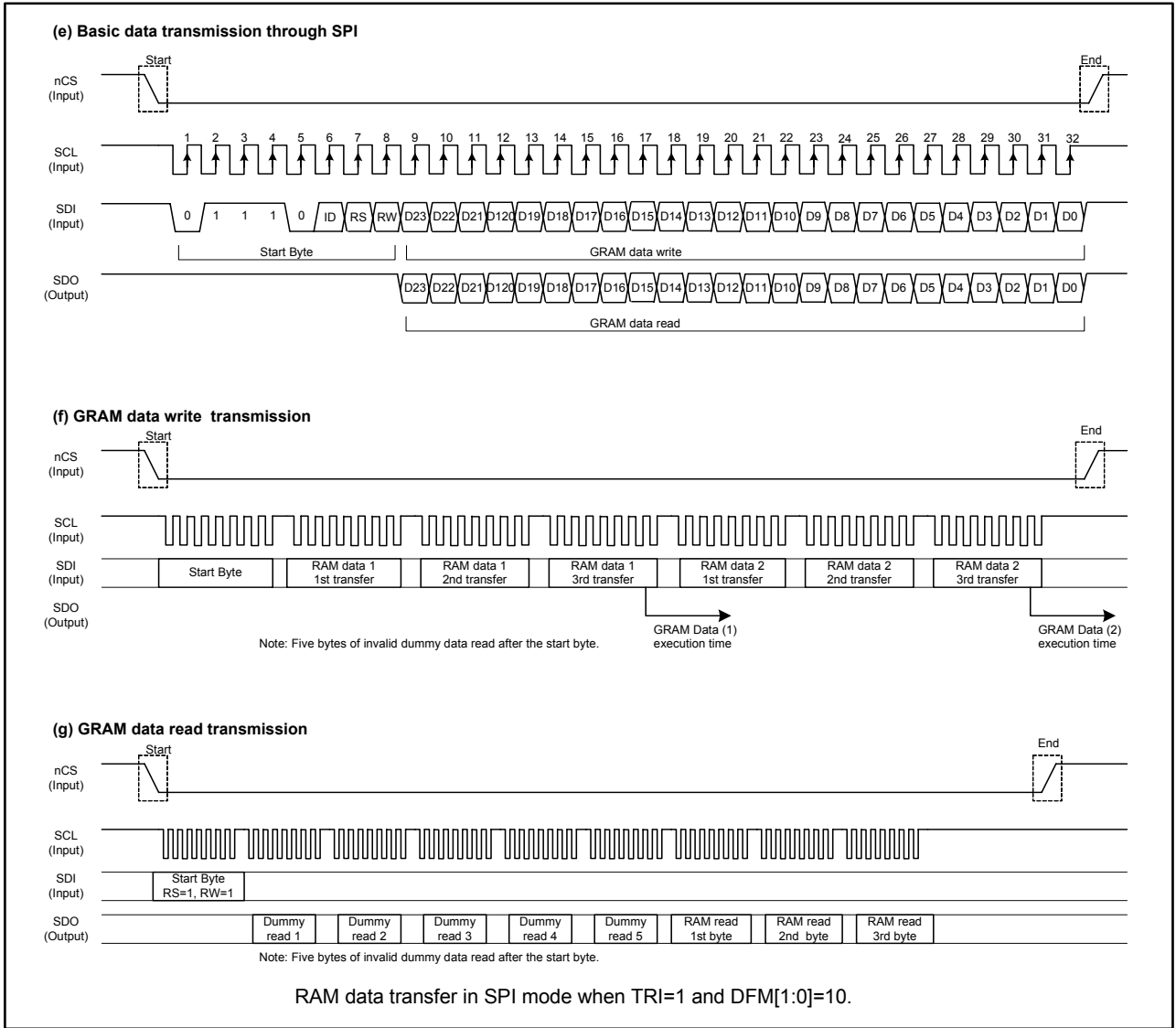


**Figure 7 Data Format of SPI Interface**





**Figure8 Data transmission through serial peripheral interface (SPI)**



**Figure9 Data transmission through serial peripheral interface (SPI), TRI="1" and DFM="10"**

## 7.4. VSYNC Interface

ILI9320 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the i80 system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".

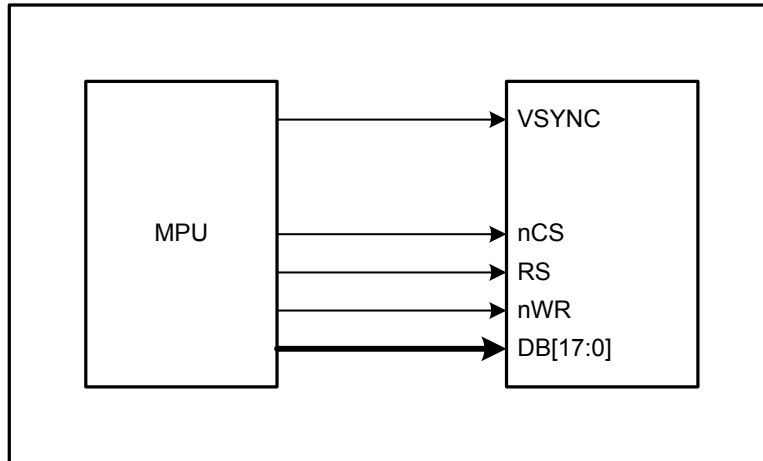


Figure10 Data transmission through VSYNC interface)

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

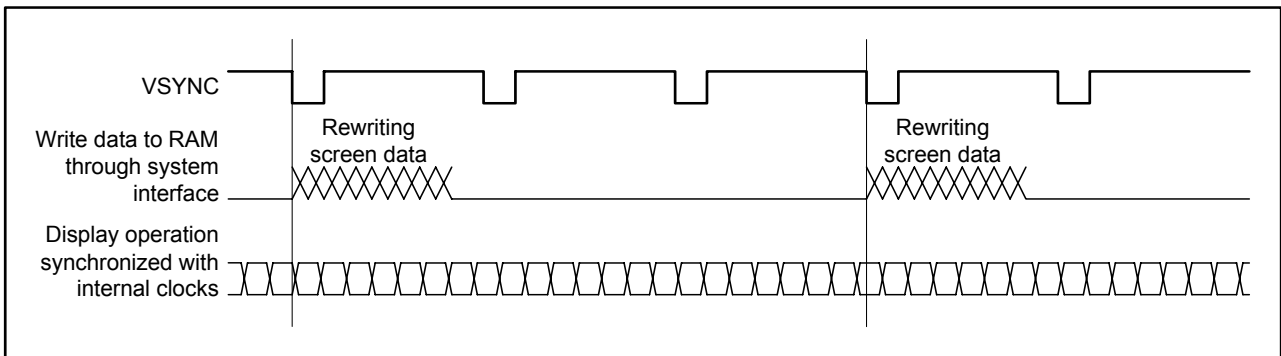
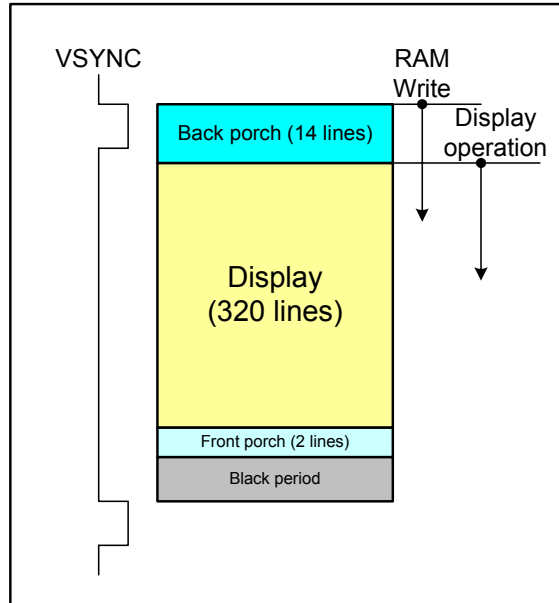


Figure11 Moving picture data transmission through VSYNC interface



**Figure12 Operation through VSYNC Interface**

The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

*Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (FP) + BackPorch (BP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.*

$$\text{Minimum RAM write speed (HZ)} > \frac{320 \times \text{DisplayLines (NL)}}{[(\text{BackPorch(BP)} + \text{DisplayLines(NL)} - \text{margins}) \times 16 \text{ (clocks)} \times 1/\text{fosc}]}$$

*Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.*

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

**[Example]**

- Display size: 240 RGB × 320 lines
- Lines: 320 lines (NL = 1000111)
- Back porch: 14 lines (BP = 1110)
- Front porch: 2 lines (FP = 0010)
- Frame frequency: 60 Hz
- Frequency fluctuation: 10%

$$\text{Internal oscillator clock (fosc.) [Hz]} = 60 \times [320 + 2 + 14] \times 16 \text{ clocks} \times (1.1/0.9) \doteq 394\text{KHz}$$

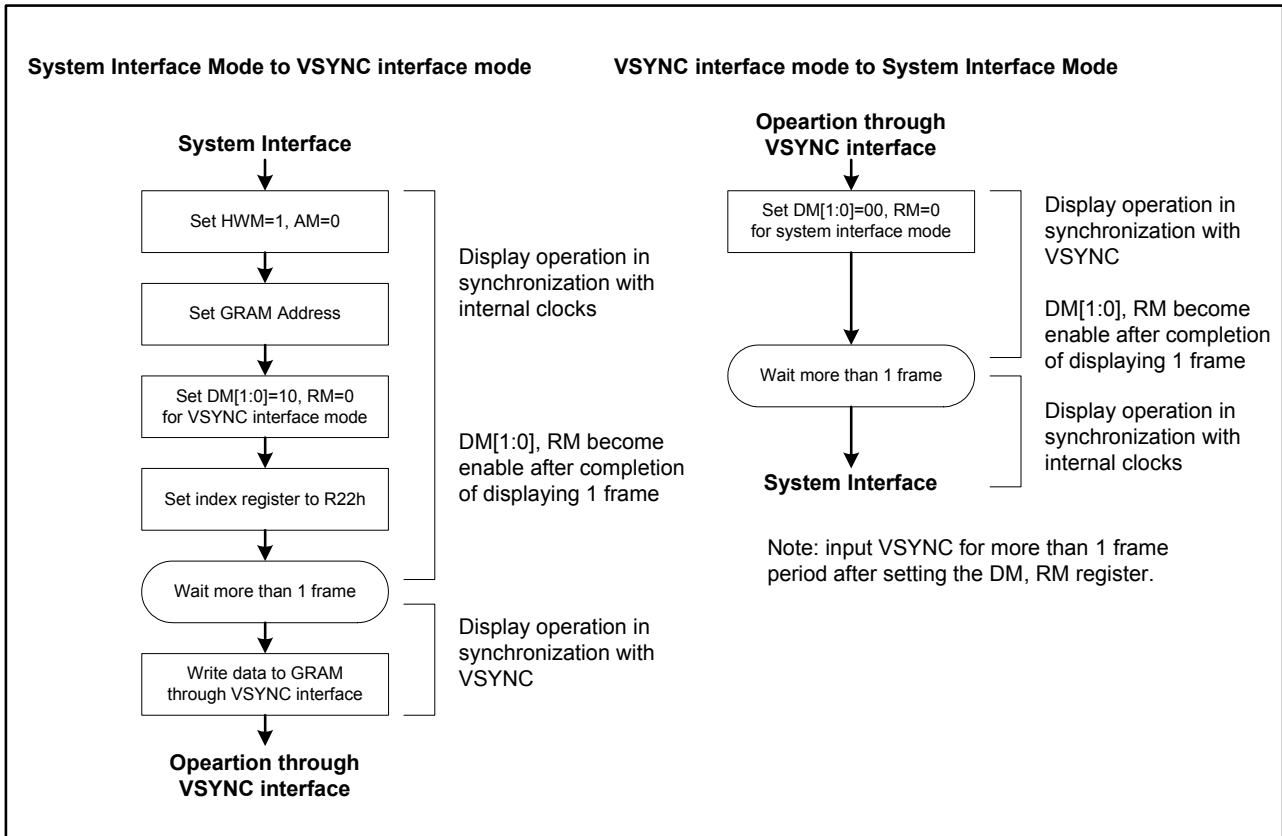
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with  $\pm 10\%$  margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

$$\text{Minimum speed for RAM writing [Hz]} > 240 \times 320 \times 394K / [(14 + 320 - 2)\text{lines} \times 16\text{clocks}] \doteq 5.7 \text{ MHz}$$

The above theoretical value is calculated based on the premise that the ILI9320 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 5.7MHz or more will guarantee the completion of GRAM write operation before the ILI9320 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

#### **Notes in using the VSYNC interface**

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to "0" to transfer display data.



**Figure13 Transition flow between VSYNC and internal clock operation modes**

## 7.5. RGB Input Interface

The RGB Interface mode is available for ILI9320 and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

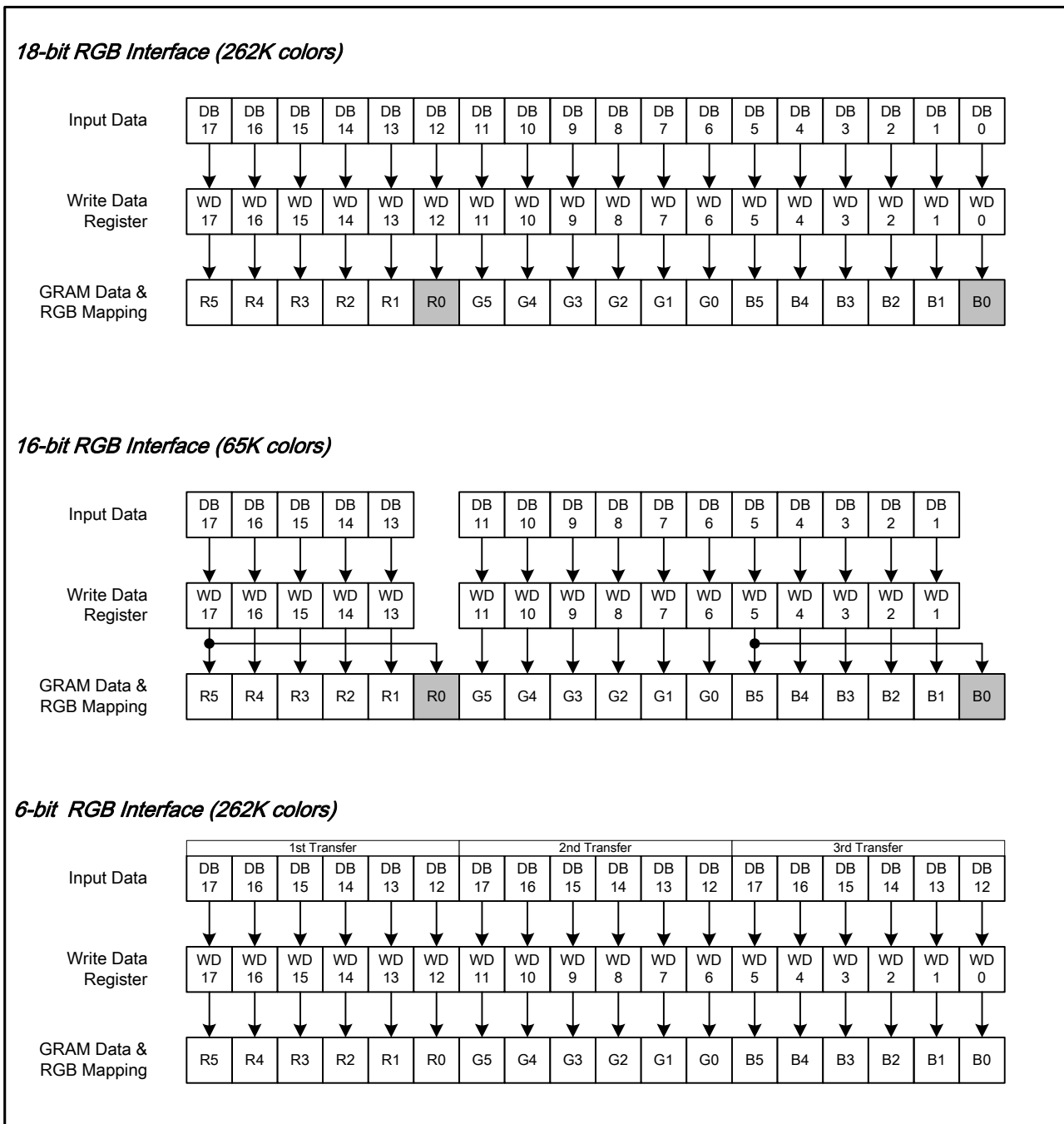
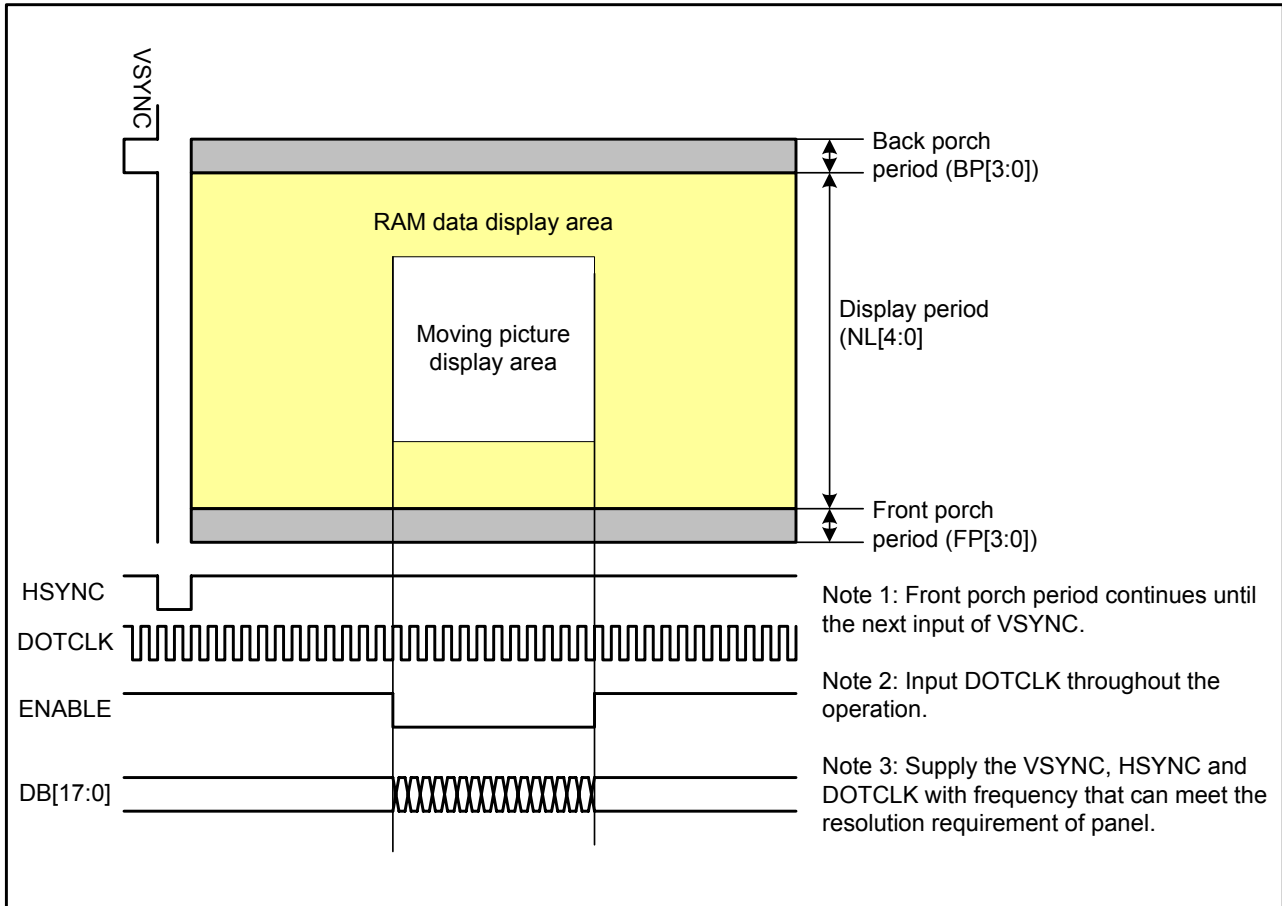


Figure14 RGB Interface Data Format

### 7.5.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM with the high-speed write function and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.

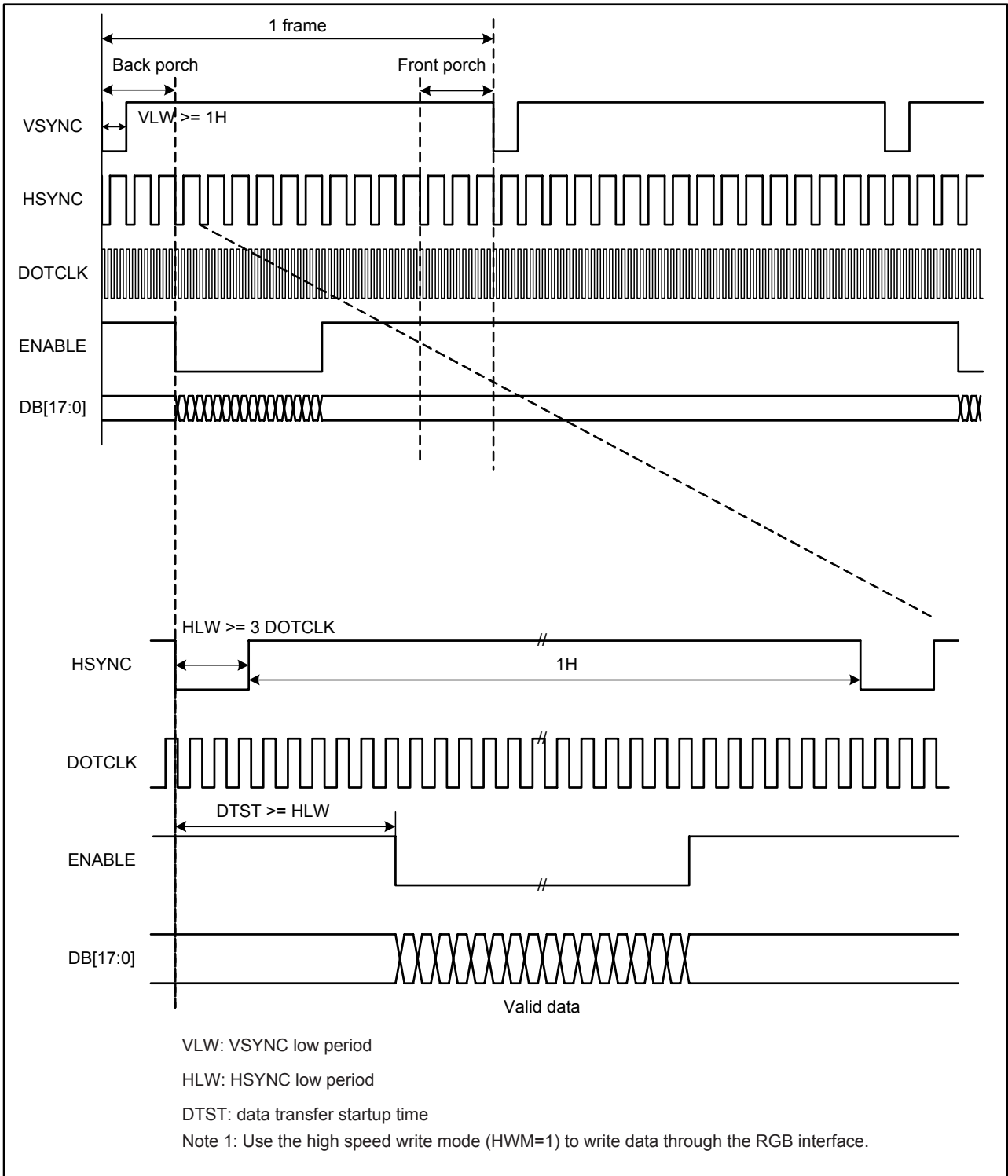


**Figure15 GRAM Access Area by RGB Interface**



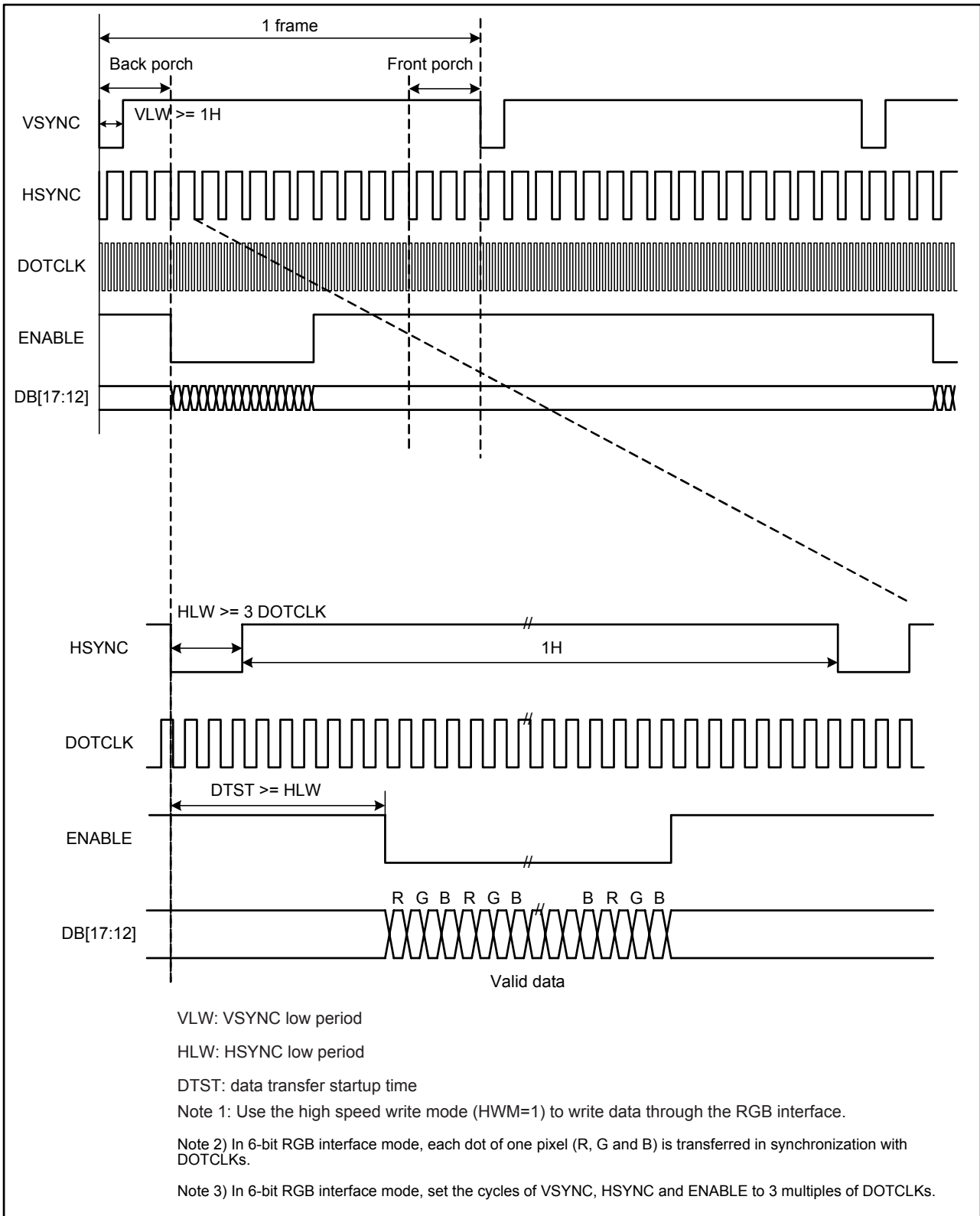
### 7.5.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as follows.



**Figure16 Timing Chart of Signals in 18-/16-bit RGB Interface Mode**

The timing chart of 6-bit RGB interface mode is shown as follows.



**Figure17 Timing chart of signals in 6-bit RGB interface mode**

### 7.5.3. Moving Picture Mode

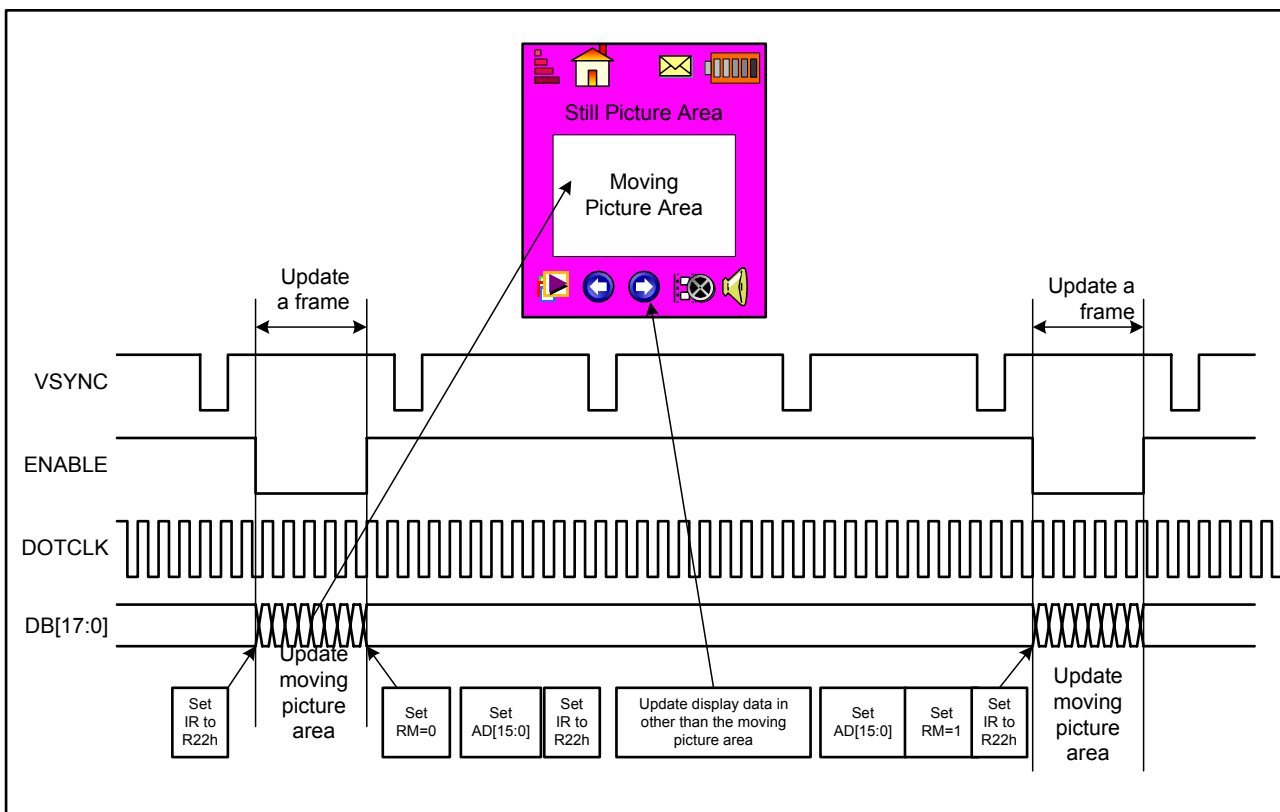
ILI9320 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

#### RAM access via a system interface in RGB-I/F mode

ILI9320 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = "0") and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

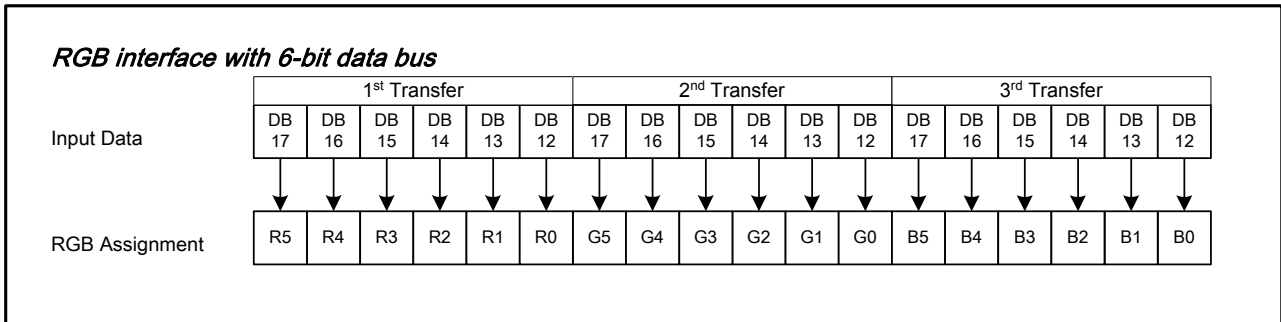
The following figure illustrates the operation of the ILI9320 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.



**Figure18 Example of update the still and moving picture**

### 7.5.4. 6-bit RGB Interface

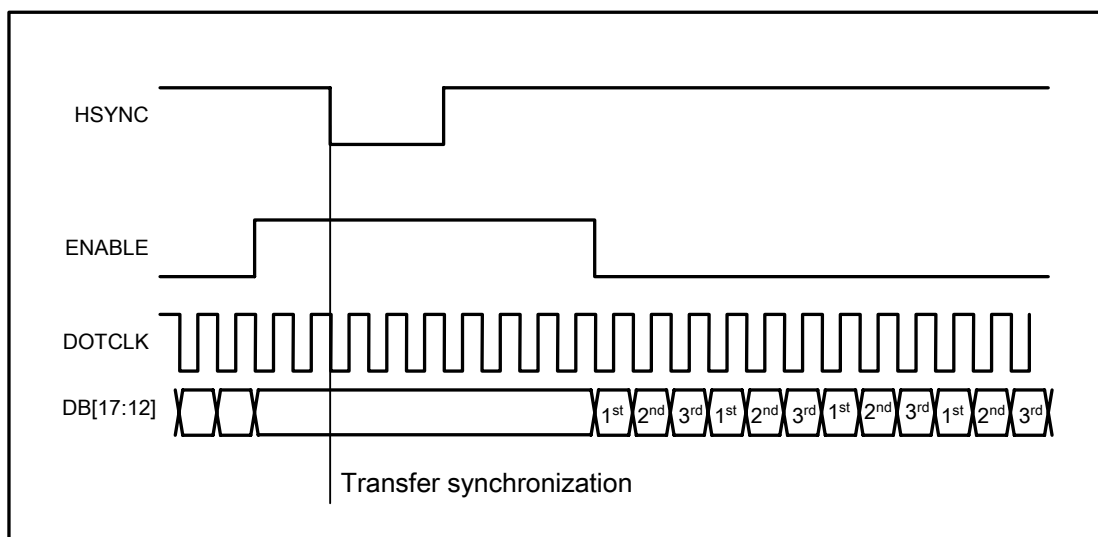
The 6-bit RGB interface is selected by setting the RIM[1:0] bits to “10”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at either IOVcc or DGND level. Registers can be set by the system interface (i80/SPI).



#### Data transfer synchronization in 6-bit RGB interface mode

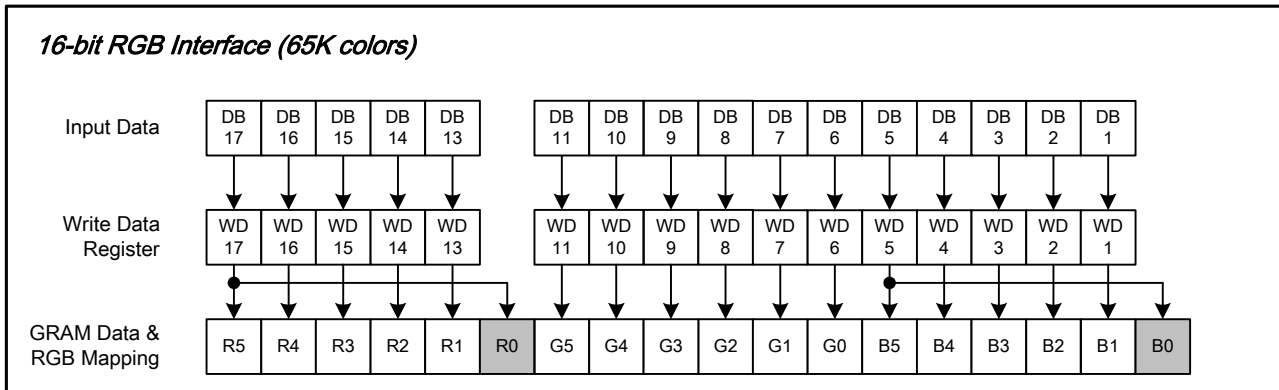
ILI9320 has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



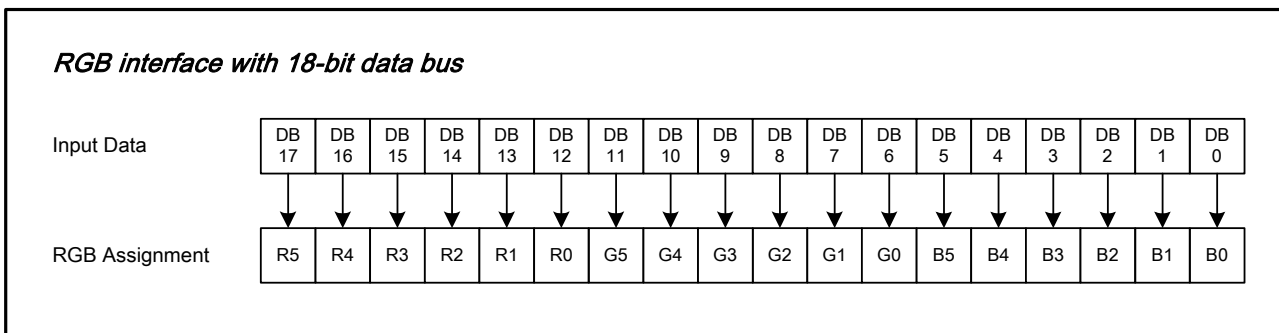
### 7.5.5. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to "01". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.



### 7.5.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to "00". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.



### Notes in using the RGB Input Interface

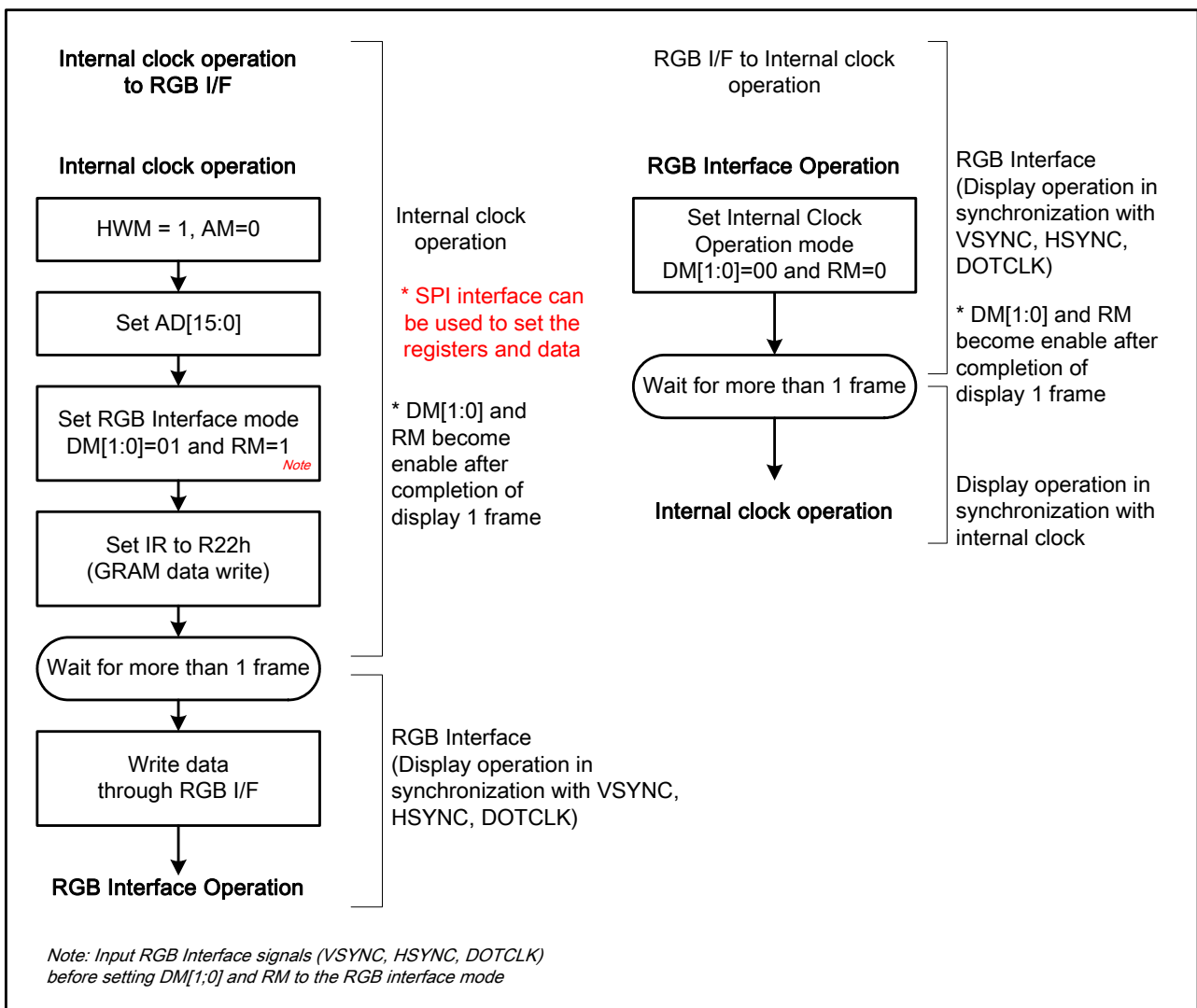
1. The following are the functions not available in RGB Input Interface mode.

Function	RGB interface	I80 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

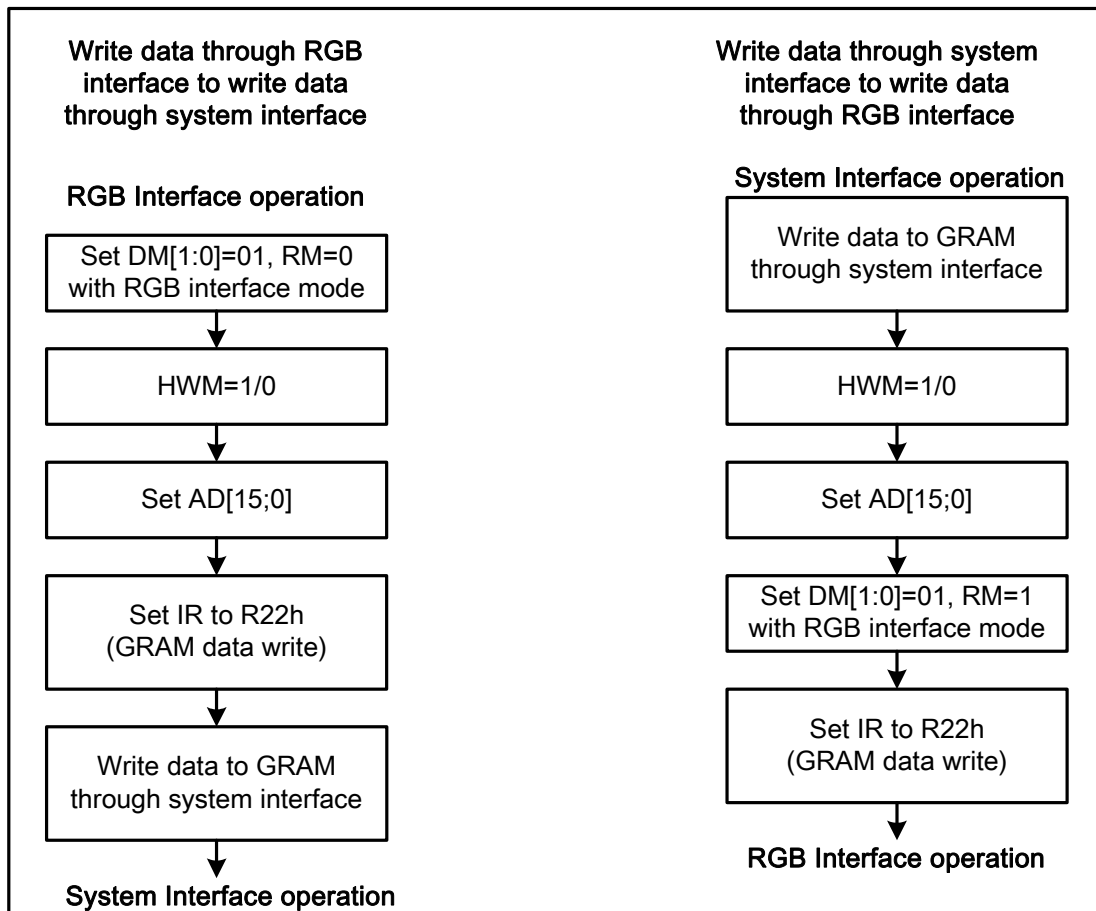
2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NO[1:0] bits (gate output non-overlap period), STD[1:0] bits (source output delay period) and EQ[1:0] bits (equalization period) are not based on the internal clock but based on DOTCLK in

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- RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
  5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
  6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
  7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
  8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.



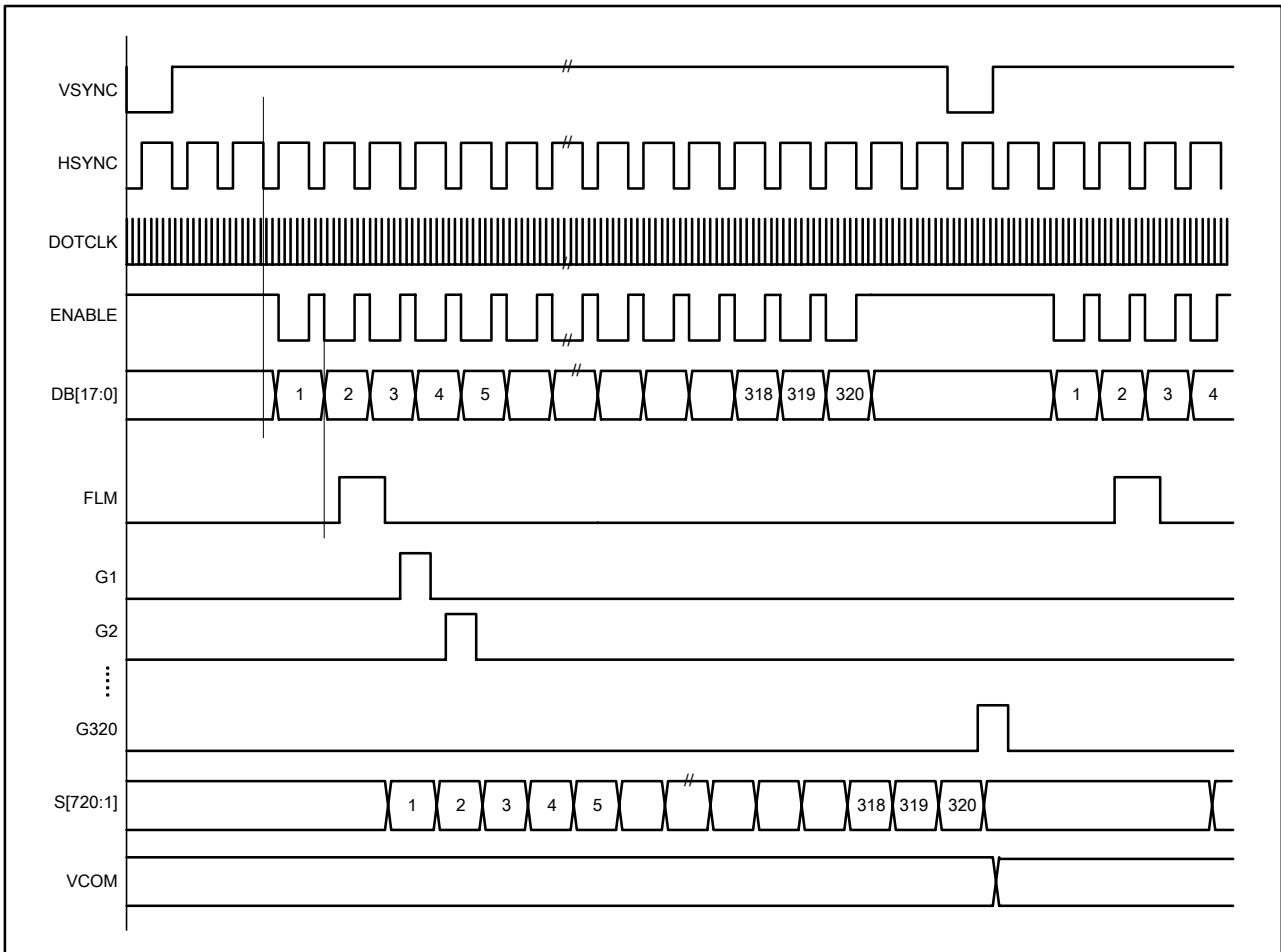
**Figure19 Internal clock operation/RGB interface mode switching**



**Figure20 GRAM access between system interface and RGB interface**

## 7.6. Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.



**Figure21 Relationship between RGB I/F signals and LCD Driving Signals for Panel**



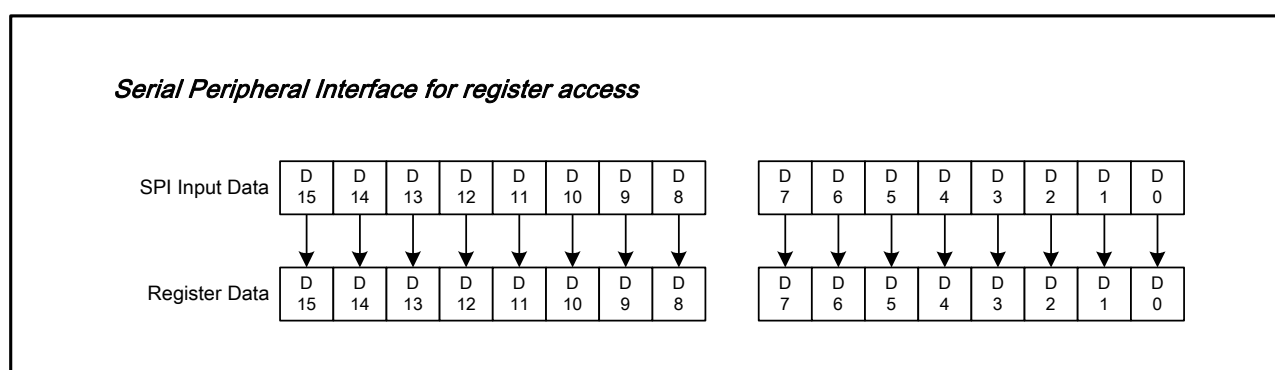
## 8. Register Descriptions

### 8.1. Registers Access

ILI9320 adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of ILI9320 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of ILI9320. The registers of the ILI9320 are categorized into the following groups.

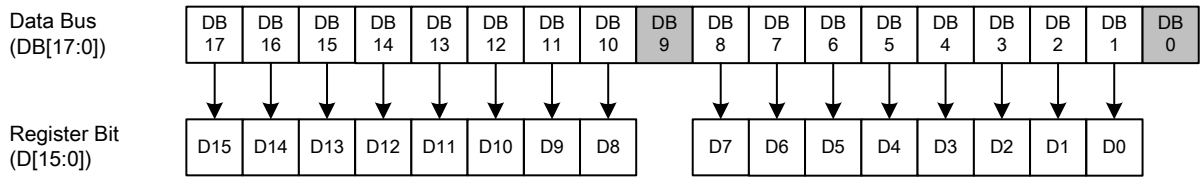
1. Specify the index of register (IR)
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address (AC)
7. Transfer data to/from the internal GRAM (R22)
8. Internal grayscale  $\gamma$ -correction (R30 ~ R39)

Normally, the display data (GRAM) is most often updated, and in order since the ILI9320 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

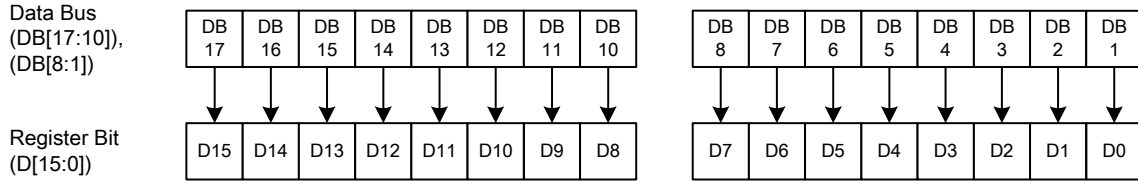


**Figure22 Register Setting with Serial Peripheral Interface (SPI)**

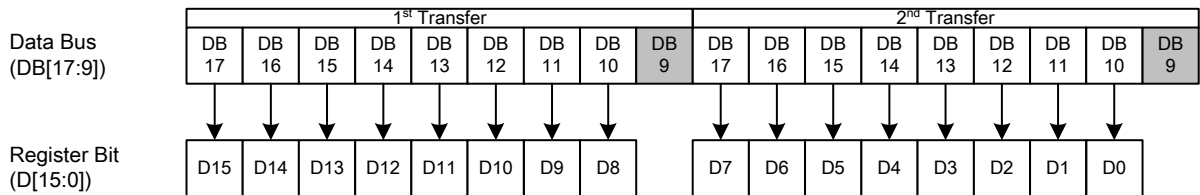
i80/M68 system 18-bit data bus interface



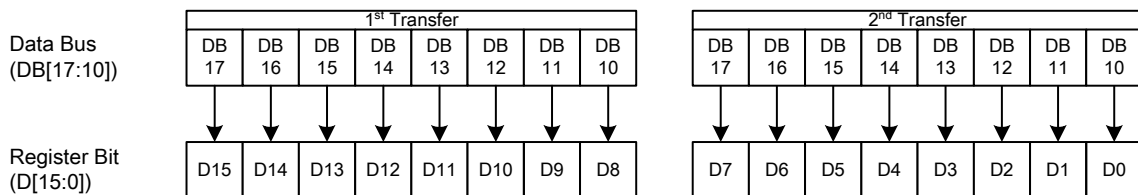
i80/M68 system 16-bit data bus interface



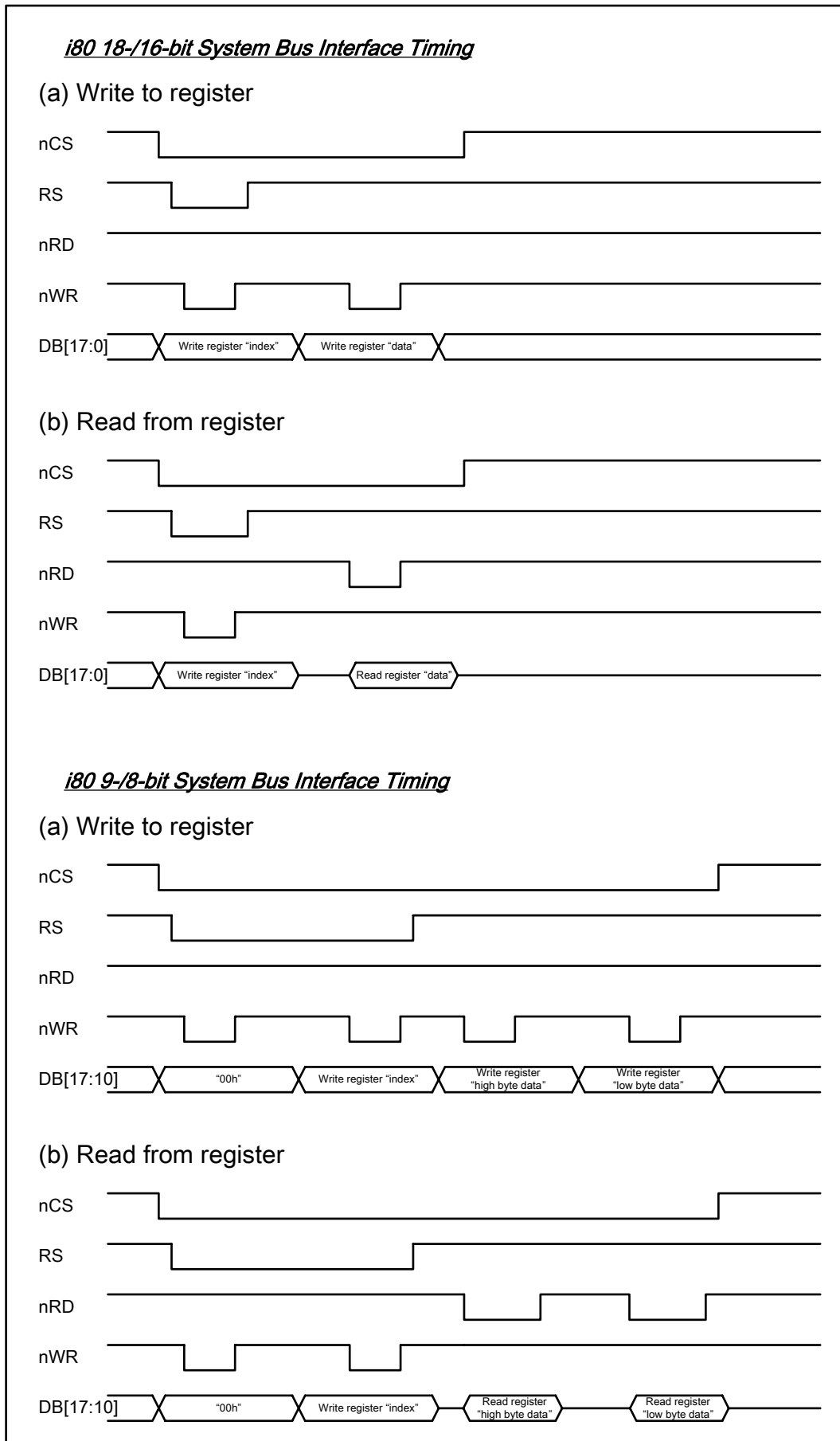
i80/M68 system 9-bit data bus interface



i80/M68 system 8-bit data bus interface/Serial peripheral interface (2/3 transmission)



**Figure23 Register setting with i80 System Interface**



**Figure 24 Register Read/Write Timing of i80 System Interface**

## 8.2. Instruction Descriptions

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
00h	Driver Code Read	R	1	1	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0
00h	Start Oscillation	W	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	OSC
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	0	BC0	EOR	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	DACKE	HWM	0	0	0	I/D1	I/D0	AM	0	0	0
04h	Resize Control	W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	BASEE	0	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	ENC2	ENC1	ENC0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	DPL	EPL
10h	Power Control 1	W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DSTB	SLP	0
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	VCMR	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1	16M_EN	Dither	0	0	0	0	0	0	EXT_R	0	FR_SEL1	FR_SEL0	0	0	0	0
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]

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No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIV11	DIV100	0	0	0	0	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0
93h	Panel Interface Control 3	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI2	MCPI1	MCPI0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
98h	Panel Interface Control 6	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2	MCPE1	MCPE0

### 8.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the address of register (R00h ~ RFFh) or RAM which will be accessed.

### 8.2.2. Status Read (RS)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

The SR bits represent the internal status of the ILI9320.

**L[7:0]** Indicates the position of driving line which is driving the TFT panel currently.

### 8.2.3. Start Oscillation (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1
R	1	1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0

Set the OSC bit as '1' to start the internal oscillator and as '0' to stop the oscillator. Wait at least 10ms to let the frequency of oscillator stable and then do the other function setting. The device code "9320" is read out when read this register.

### 8.2.4. Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

**SS:** Select the shift direction of outputs from the source driver.

When SS = 0, the shift direction of outputs is from S1 to S720

When SS = 1, the shift direction of outputs is from S720 to S1.

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

**When changing SS or BGR bits, RAM data must be rewritten.**

**SM:** Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		<p>G1, G2, G3, G4, ..., G316 G317, G318, G319, G320</p>
0	1		<p>G320, G319, G318, ..., G6, G5, G4, G3, G2, G1</p>
1	0		<p>G1, G3, G5, G7, ..., G311 G313, G315, G317, G319</p> <p>G2, G4, G6, G8, ..., G312 G314, G316, G318, G320</p>
1	1		<p>G320, G318, G316, ..., G10, G8, G6, G4, G2</p> <p>G319, G317, G315, ..., G9, G7, G5, G3, G1</p>

**8.2.5. LCD Driving Wave Control (R02h)**

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0

**.B/C** 0 : Frame/Field inversion  
1 : Line inversion

**EOR:** EOR = 1 and B/C=1 to set the line inversion.

**8.2.6. Entry Mode (R03h)**

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0

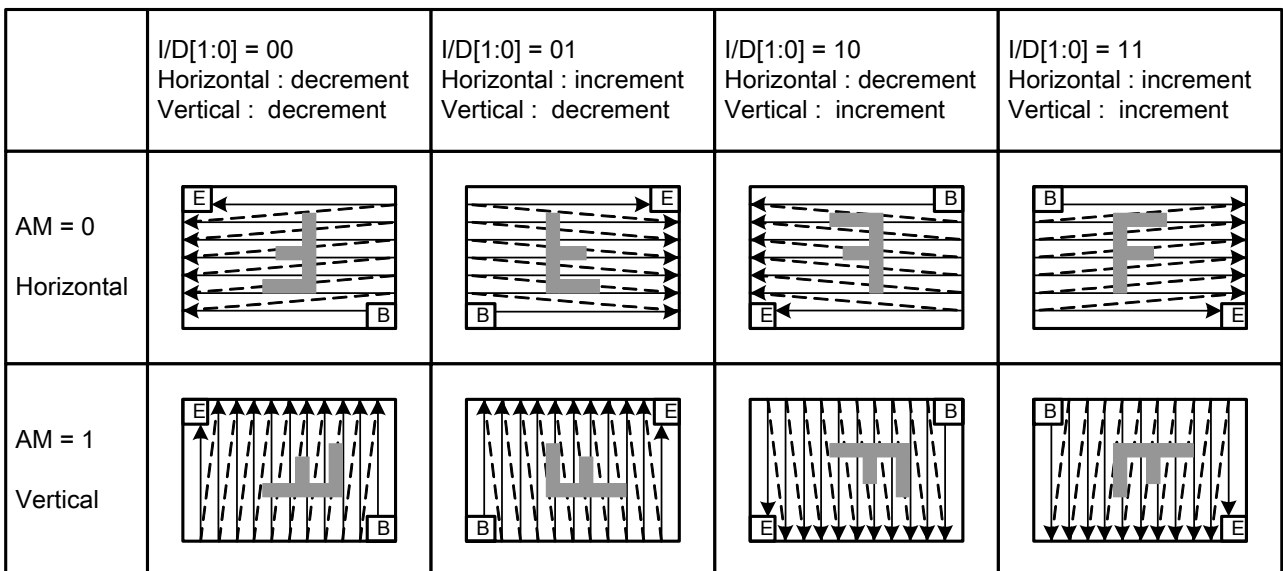
**AM** Control the GRAM update direction.

When AM = "0", the address is updated in horizontal writing direction.

When AM = "1", the address is updated in vertical writing direction.

When a window area is set by registers R16h and R17h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

**I/D[1:0]** Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.



**Figure25 GRAM Access Direction Setting**

**ORG** Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.

ORG = "0": The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.



ORG = "1": The original address "00000h" moves according to the I/D[1:0] setting.

Notes: 1. When ORG=1, only the origin address address"00000h" can be set in the RAM address set registers R20h, and R21h.

2. In RAM read operation, make sure to set ORG=0.

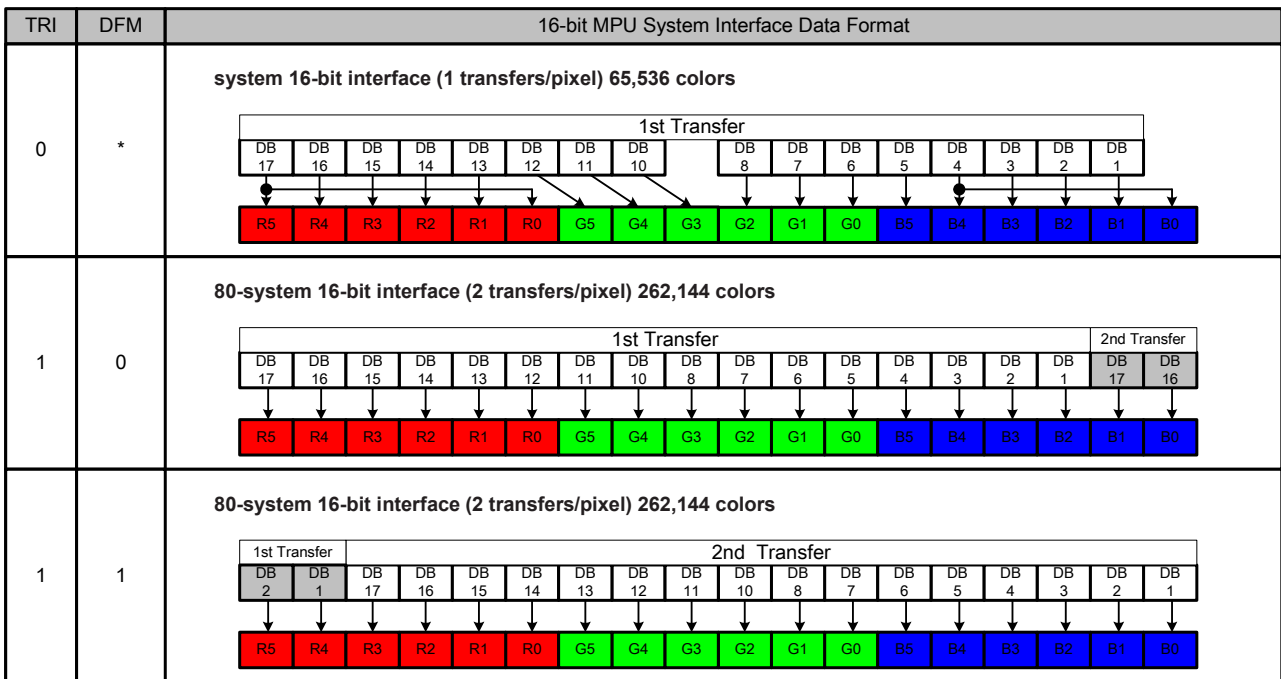
**BGR** Swap the R and B order of written data.

BGR="0": Follow the RGB order to write the pixel data.

BGR="1": Swap the RGB data to BGR in writing into GRAM.

**TRI** When TRI = "1", data are transferred to the internal RAM in 8-bit x 3 transfers mode via the 8-bit interface. It is also possible to send data via the 16-bit interface or SPI in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI = "0".

**DFM** Set the mode of transferring data to the internal RAM when TRI = "1". See the following figures for details.



**Figure26 16-bit MPU System Interface Data Format**

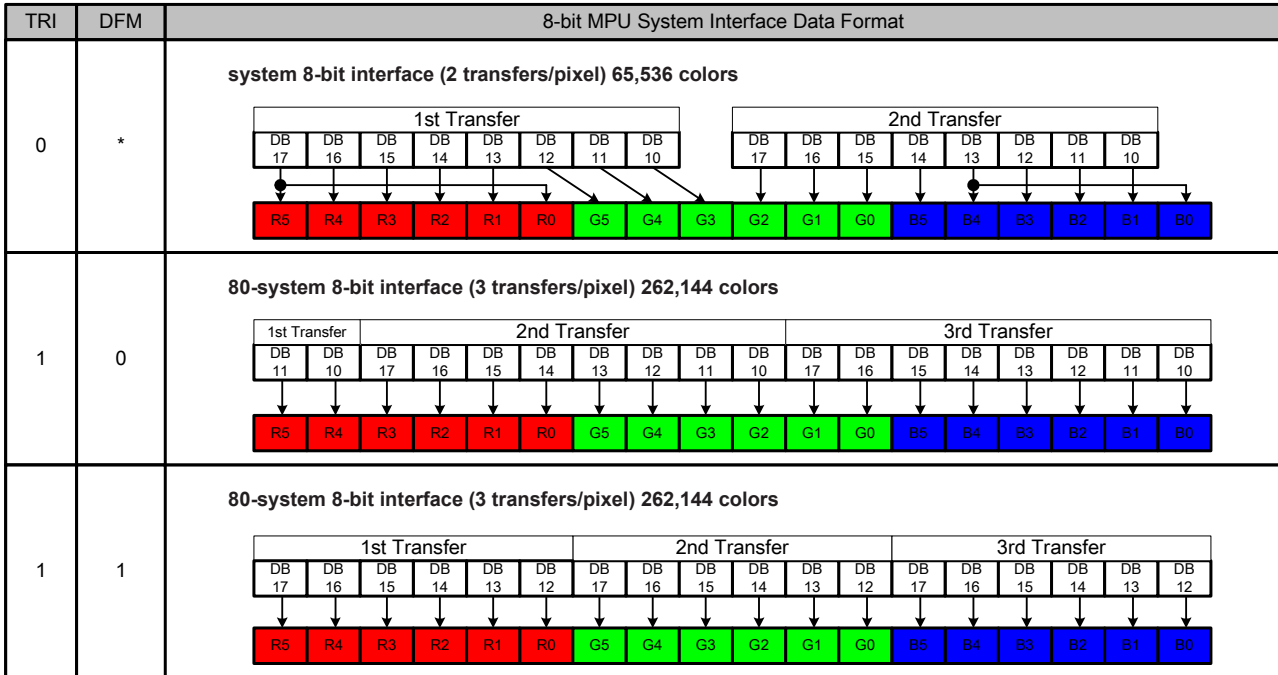


Figure27 8-bit MPU System Interface Data Format

### 8.2.7. Resizing Control Register (R04h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0

**RSZ[1:0]** Sets the resizing factor.

When the RSZ bits are set for resizing, the ILI9320 writes the data according to the resizing factor so that the original image is displayed in horizontal and vertical dimensions, which are contracted according to the factor respectively. See “Resizing function”.

**RCH[1:0]** Sets the number of remainder pixels in horizontal direction when resizing a picture.

By specifying the number of remainder pixels by RCH bits, the data can be transferred without taking the remainder pixels into consideration. Make sure that RCH = 2’h0 when not using the resizing function (RSZ = 2’h0) or there are no remainder pixels.

**RCV[1:0]** Sets the number of remainder pixels in vertical direction when resizing a picture.

By specifying the number of remainder pixels by RCV bits, the data can be transferred without taking the remainder pixels into consideration. Make sure that RCV = 2’h0 when not using the resizing function (RSZ = 2’h0) or there are no remainder pixels.

RSZ[1:0]	Resizing factor
00	No resizing (x1)
01	x 1/2
10	Setting prohibited
11	x 1/4

RCH[1:0]	Number of remainder Pixels in Horizontal Direction
00	0 pixel*

01	1 pixel
10	2 pixel
11	3 pixel

RCV[1:0]	Number of remainder Pixels in Vertical Direction
00	0 pixel*
01	1 pixel
10	2 pixel
11	3 pixel

\*1 pixel = 1RGB

### 8.2.8. Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	PTDE1	PTDE0	0	0	BASEE	0	0	0	GON	DTE	CL	0	D1	D0

**D[1:0]** Set D[1:0]="11" to turn on the display panel, and D[1:0]="00" to turn off the display panel.

A graphics display is turned on the panel when writing D1 = "1", and is turned off when writing D1 = "0".

When writing D1 = "0", the graphics display data is retained in the internal GRAM and the ILI9320 displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D[1:0] = "01", the ILI9320 continues internal display operation. When the display is turned off by setting D[1:0] = "00", the ILI9320 internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF.

D1	D0	BASEE	Source, VCOM Output	ILI9320 internal operation
0	0	0	GND	Halt
0	1	1	GND	Operate
1	0	0	Non-lit display	Operate
1	1	0	Non-lit display	Operate
1	1	1	Base image display	Operate

Note: 1. data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

- The internal state of the ILI9320 in standby mode become the same as when D[1:0] = "00". This does not mean the D[1:0] setting is changed when setting the standby mode.
- The D[1:0] setting is valid on both 1<sup>st</sup> and 2<sup>nd</sup> displays.
- The non-lit display level from the source output pins is determined by instruction (PTS).

**CL** When CL = "1", the 8-color display mode is selected.

CL	Colors
0	262,144
1	8

**GON and DTE** Set the output level of gate driver G1 ~ G320 as follows

GON	DTE	G1 ~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
<b>1</b>	<b>1</b>	<b>Normal Display</b>

**BASEE**

Base image display enable bit. When BASEE = “0”, no base image is displayed. The ILI9320 drives liquid crystal at non-lit display level or displays only partial images. When BASEE = “1”, the base image is displayed. The D[1:0] setting has higher priority over the BASEE setting.

**PTDE[1:0]**

Partial image 2 and Partial image 1 enable bits

PTDE1/0 = 0: turns off partial image. Only base image is displayed.

PTDE1/0 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

**8.2.9. Display Control 2 (R08h)**

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

**FP[3:0]/BP[3:0]**

The FP[3:0] and BP[3:0] bits specify the line number of front and back porch periods respectively.

When setting the FP[3:0] and BP[3:0] value, the following conditions shall be met:

$BP + FP \leq 16$  lines

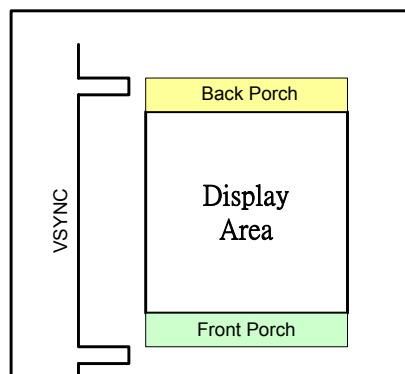
**$FP \geq 2$  lines**

**$BP \geq 2$  lines**

Set the BP[3:0] and FP[3:0] bits as below for each operation modes

Operation Mode	BP	FP	BP+FP
<b>180 System Interface Operation Mode</b>	BP $\geq$ 2 lines	FP $\geq$ 2 lines	FP +BP $\leq$ 16 lines
<b>RGB interface Operation</b>	BP $\geq$ 2 lines	FP $\geq$ 2 lines	FP +BP $\leq$ 16 lines
<b>VSYNC interface Operation</b>	BP $\geq$ 2 lines	FP $\geq$ 2 lines	FP +BP = 16 lines

FP[3:0]	Number of lines for Front Porch
BP[3:0]	Number of lines for Back Porch
0000	Setting Prohibited
0001	Setting Prohibited
0010	2 lines
0011	3 lines
0100	4 lines
0101	5 lines
0110	6 lines
0111	7 lines
1000	8 lines
1001	9 lines



1010	10 lines
1011	11 lines
1100	12 lines
1101	13 lines
1110	14 lines
1111	Setting Prohibited

**8.2.10. Display Control 3 (R09h)**

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

**ISC[3:0]:** Specify the scan cycle interval of gate driver in non-display area when PTG[1:0]="10" to select interval scan. Then scan cycle is set as odd number from 0~31 frame periods. The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f <sub>FLM</sub> =60 Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frame	50ms
0	0	1	0	5 frame	84ms
0	0	1	1	7 frame	117ms
0	1	0	0	9 frame	150ms
0	1	0	1	11 frame	184ms
0	1	1	0	13 frame	217ms
0	1	1	1	15 frame	251ms
1	0	0	0	17 frame	284ms
1	0	0	1	19 frame	317ms
1	0	1	0	21 frame	351ms
1	0	1	1	23 frame	384ms
1	1	0	0	25 frame	418ms
1	1	0	1	27 frame	451ms
1	1	1	0	29 frame	484ms
1	1	1	1	31 frame	518ms

**PTG[1:0]** Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	Vcom output
0	0	Normal scan	Set with the PTS[2:0] bits	VcomH/VcomL
0	1	Setting Disabled	-	-
1	0	Interval scan	Set with the PTS[2:0] bits	VcomH/VcomL
1	1	Setting Disabled	-	-

**PTS[2:0]**

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

PTS[2:0]	Source output level	Grayscale amplifier	Step-up clock frequency
----------	---------------------	---------------------	-------------------------

	Positive polarity	Negative polarity	in operation	
000	V63	V0	V63 to V0	Register Setting(DC1, DC0)
001	Setting Prohibited	Setting Prohibited	-	-
010	GND	GND	V63 to V0	Register Setting(DC1, DC0)
011	Hi-Z	Hi-Z	V63 to V0	Register Setting(DC1, DC0)
100	V63	V0	V63 and V0	1/2 frequency setting by DC1, DC0
101	Setting Prohibited	Setting Prohibited	-	-
110	GND	GND	V63 and V0	1/2 frequency setting by DC1, DC0
111	Hi-Z	Hi-Z	V63 and V0	1/2 frequency setting by DC1, DC0

- Notes: 1. The power efficiency can be improved by halting grayscale amplifiers and slowing down the step-up clock frequency only in non-display drive period.  
2. The gate output level in non-lit display area drive period is determined by PTG[1:0].

### 8.2.11. Display Control 4 (R0Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0

**FMI[2:0]** Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

**FMARKOE** When FMARKOE=1, ILI9320 starts to output FMARK signal in the output interval set by FMI[2:0] bits.

FMI[2:0]	Output Interval
000	1 frame
001	2 frame
011	4 frame
101	6 frame
Others	Setting disabled

### 8.2.12. RGB Display Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	ENC2	ENC1	ENC0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

**RIM[1:0]** Select the RGB interface data width.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (1 transfer/pixel), DB[17:0]
0	1	16-bit RGB interface (1 transfer/pixel), DB[17:13] and DB[11:1]
1	0	6-bit RGB interface (3 transfers/pixel), DB[17:12]
1	1	Setting disabled

Note1: Registers are set only by the system interface.

Note2: Be sure that one pixel (3 dots) data transfer finished when interface switch.

**DM[1:0]** Select the display operation mode.

DM1	DM0	Display Interface
0	0	Internal system clock
0	1	RGB interface
1	0	VSYNC interface

1	1	Setting disabled
---	---	------------------

The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

**RM** Select the interface to access the GRAM.

Set RM to “1” when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0])
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
Rewrite still picture area while RGB interface Displaying moving pictures.		System interface (RM = 0)	RGB interface (DM[1:0] = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Note 1: Registers are set only via the system interface or SPI interface.

Note 2: Refer to the flowcharts of “RGB Input Interface” section for the mode switch.

**ENC[2:0]** Set the GRAM write cycle through the RGB interface

ENC[2:0]	GRAM Write Cycle (Frame periods)
000	1 Frame
001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

### 8.2.13. Frame Marker Position (R0Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0

**EMP[8:0]** Sets the output position of frame cycle (frame marker).

When FMP[8:0]=0, a high-active pulse FMARK is output at the start of back porch period for one display line period (1H).

Make sure the  $9'h000 \leq FMP \leq BP+NL+FP$

FMP[8:0]	FMARK Output Position
9'h000	0 <sup>th</sup> line
9'h001	1 <sup>st</sup> line
9'h002	2 <sup>nd</sup> line

9'h003	3 <sup>rd</sup> line
.	.
.	.
9'h175	373 <sup>rd</sup> line
9'h176	374 <sup>th</sup> line
9'h177	375 <sup>th</sup> line

### 8.2.14. RGB Display Interface Control 2 (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

**DPL:** Sets the signal polarity of the DOTCLK pin.

DPL = "0" The data is input on the rising edge of DOTCLK

DPL = "1" The data is input on the falling edge of DOTCLK

**EPL:** Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".

EPL = "1" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".

**HSPL:** Sets the signal polarity of the SYNC pin.

HSPL = "0" Low active

HSPL = "1" High active

**VSPL:** Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active

VSPL = "1" High active

### 8.2.15. Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DSTB	SLP	0

**SLP:** When SLP = 1, ILI9320 enters the sleep mode and the display operation stops except the RC oscillator to reduce the power consumption. In the sleep mode, the GRAM data and instructions cannot be updated except the following two instructions.

- a. Exit sleep mode (SLP = "0")
- b. Start oscillation

**DSTB:** When DSTB = 1, the ILI9320 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the ILI9320 enters the deep standby mode, and they must be reset after exiting deep standby mode.



**AP[2:0]:** Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = "000" to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	In LCD drive power supply amplifiers	In Source driver amplifiers
000	Halt operational amplifiers and step-up circuits	Halt
001	0.5	0.62
010	0.75	0.71
011	1	1
100		
101	0.5	0.62
110	0.75	0.71
111	1	1

**SAP:** Source Driver output control

SAP=0, Source driver output is disabled.

SAP=1, Source driver output is enabled.

When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

**APE:** Power supply enable bit.

Set APE = "1" to start the generation of power supply according to the power supply startup sequence.

**BT[3:0]:** Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[3:0]	DDVDH	VCL	VGH	VGL
4'h0	Vci1 x 2	- Vci1	Vci1 x 6	- Vci1 x 5
4'h1	Vci1 x 2	- Vci1	Vci1 x 8	- Vci1 x 4
4'h2				- Vci1 x 3
4'h3	Vci1 x 2	- Vci1	Vci1 x 7	- Vci1 x 5
4'h4				- Vci1 x 4
4'h5				- Vci1 x 3
4'h6	Vci1 x 2	- Vci1	Vci1 x 6	- Vci1 x 4
4'h7				- Vci1 x 3
4'h8	Vci1 x 3	- Vci1	Vci1 x 9	- Vci1 x 7
4'h9	Vci1 x 3	- Vci1	Vci1 x 12	- Vci1 x 6
4'hA				- Vci1 x 4
4'hB				- Vci1 x 7
4'hC	Vci1 x 3	- Vci1	Vci1 x 10	- Vci1 x 6
4'hD				- Vci1 x 4
4'hE	Vci1 x 3	- Vci1	Vci1 x 9	- Vci1 x 6
4'hF				- Vci1 x 4

Notes: 1. Connect capacitors to the capacitor connection pins when generating DDVDH, VGH, VGL and VCL levels.

2. Make sure DDVDH = 6.0V (max.), VGH = 15.0V (max.), VGL = - 12.5V (max) and VCL= -3.0V (max.)

### 8.2.16. Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

**VC[2:0]** Sets the ratio factor of VciLVL to generate the reference voltages VciOUT and Vci1.

VC2	VC1	VC0	VciOUT reference voltage	Vci1 voltage
0	0	0	0.94 x Vci	
0	0	1	0.89 x Vci	
0	1	0	Setting disabled	
0	1	1	Setting disabled	
1	0	0	0.76 x Vci	
1	0	1	Setting disabled	
1	1	0	Setting disabled	
1	1	1	1.0 x Vci	

**DC0[2:0]:** Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

**DC1[2:0]:** Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC02	DC01	DC00	Step-up circuit1 step-up frequency ( $f_{DCDC1}$ )	DC12	DC11	DC10	Step-up circuit2 step-up frequency ( $f_{DCDC2}$ )
0	0	0	Fosc	0	0	0	Fosc / 16
0	0	1	Fosc / 2	0	0	1	Fosc / 32
0	1	0	Fosc / 4	0	1	0	Fosc / 64
0	1	1	Fosc / 8	0	1	1	Fosc / 128
1	0	0	Fosc / 16	1	0	0	Fosc / 256
1	0	1	Setting disabled	1	0	1	Setting disabled
1	1	0	Halt step-up circuit 1	1	1	0	Halt step-up circuit 2
1	1	1	Setting disabled	1	1	1	Setting disabled

Note: Be sure  $f_{DCDC1} \geq f_{DCDC2}$  when setting DC0[2:0] and DC1[2:0].

### 8.2.17. Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	VCMR	0	0	0	PON	VRH3	VRH2	VRH1	VRH0

**VRH[3:0]** Set the amplifying rate (1.6 ~ 1.9) of VciLVL applied to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VRH3	VRH2	VRH1	VRH0	VREG1OUT	VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt	1	0	0	0	VciLVL x 1.60
0	0	0	1	Setting inhibited	1	0	0	1	VciLVL x 1.65
0	0	1	0	Setting inhibited	1	0	1	0	VciLVL x 1.70
0	0	1	1	Setting inhibited	1	0	1	1	VciLVL x 1.75
0	1	0	0	Setting inhibited	1	1	0	0	VciLVL x 1.80
0	1	0	1	Setting inhibited	1	1	0	1	VciLVL x 1.85
0	1	1	0	Setting inhibited	1	1	1	0	VciLVL x 1.90
0	1	1	1	Setting inhibited	1	1	1	1	Setting inhibited

Make sure that VC and VRH setting restriction:  $VREG1OUT \leq (DDVDH - 0.5)V$ .

**PON:** Control ON/OFF of circuit3 (VGL) output.

PON=0	VGL output is disable
PON=1	VGL output is enable

**VCMR:** Selects either external resistor (VcomR) or internal electric volume (VCM) to set the electrical potential of VcomH (Vcom center voltage level).

VCMR = 0 → Using the external variable resistor to adjust the VcomH voltage level

VCMR = 1 → Using the Internal electronic volume (VCM[4:0]) to adjust the VcomH voltage level.

### 8.2.18. Power Control 4 (R13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

**VDV[4:0]** Select the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.70 to 1.24 x VREG1OUT .

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude	VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	VREG1OUT x 0.70	1	0	0	0	0	VREG1OUT x 0.87
0	0	0	0	1	VREG1OUT x 0.72	1	0	0	0	1	VREG1OUT x 0.89
0	0	0	1	0	VREG1OUT x 0.74	1	0	0	1	0	VREG1OUT x 0.92
0	0	0	1	1	VREG1OUT x 0.76	1	0	0	1	1	VREG1OUT x 0.94
0	0	1	0	0	VREG1OUT x 0.78	1	0	1	0	0	VREG1OUT x 0.96
0	0	1	0	1	VREG1OUT x 0.80	1	0	1	0	1	VREG1OUT x 0.99
0	0	1	1	0	VREG1OUT x 0.82	1	0	1	1	0	VREG1OUT x 1.01
0	0	1	1	1	VREG1OUT x 0.84	1	0	1	1	1	VREG1OUT x 1.04
0	1	0	0	0	VREG1OUT x 0.86	1	1	0	0	0	VREG1OUT x 1.06
0	1	0	0	1	VREG1OUT x 0.88	1	1	0	0	1	VREG1OUT x 1.09
0	1	0	1	0	VREG1OUT x 0.90	1	1	0	1	0	VREG1OUT x 1.11
0	1	1	1	1	VREG1OUT x 0.92	1	1	1	1	1	VREG1OUT x 1.14
0	1	1	0	0	VREG1OUT x 0.94	1	1	1	0	0	VREG1OUT x 1.16
0	1	1	0	1	VREG1OUT x 0.96	1	1	1	0	1	VREG1OUT x 1.19
0	1	1	1	0	VREG1OUT x 0.98	1	1	1	1	0	VREG1OUT x 1.21
0	1	1	1	1	VREG1OUT x 1.00	1	1	1	1	1	VREG1OUT x 1.24

Set VDV[4:0] to let Vcom amplitude less than 6V.

### 8.2.19. GRAM Horizontal/Vertical Address Set (R20h, R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

**AD[16:0]** Set the initial value of address counter (AC).

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The address counter (AC) is automatically updated in accordance to the setting of the AM, I/D bits as data is written to the internal GRAM. The address counter is not automatically updated when read data from the internal GRAM.

AD[16:0]	GRAM Data Map
17'h00000 ~ 17'h000EF	1 <sup>st</sup> line GRAM Data
17'h00100 ~ 17'h001EF	2 <sup>nd</sup> line GRAM Data
17'h00200 ~ 17'h002EF	3 <sup>rd</sup> line GRAM Data
17'h00300 ~ 17'h003EF	4 <sup>th</sup> line GRAM Data
17'h13D00 ~ 17' h13DEF	318 <sup>th</sup> line GRAM Data
17'h13E00 ~ 17' h13EEF	319 <sup>th</sup> line GRAM Data
17'h13F00 ~ 17'h13FEF	320 <sup>th</sup> line GRAM Data

Note1: When the RGB interface is selected (RM = "1"), the address AD[16:0] is set to the address counter every frame on the falling edge of VSYNC.

Note2: When the internal clock operation or the VSYNC interface mode is selected (RM = "0"), the address AD[16:0] is set to address counter when update register R21.

### 8.2.20. Write Data to GRAM (R22h)

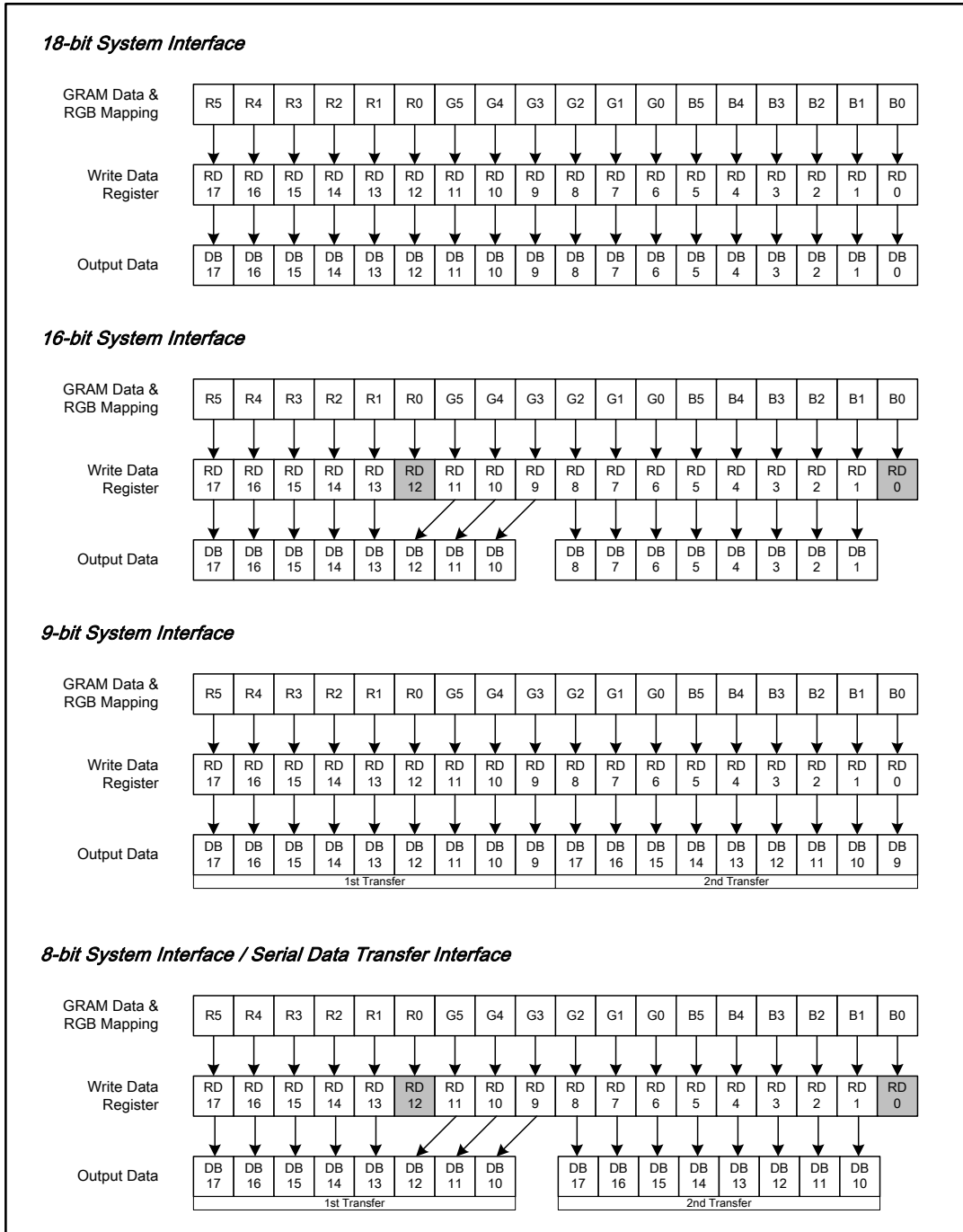
R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data (WD[17:0], the DB[17:0] pin assignment differs for each interface.																	

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

### 8.2.21. Read Data from GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	RAM Read Data (RD[17:0], the DB[17:0] pin assignment differs for each interface.																	

**RD[17:0]** Read 18-bit data from GRAM through the read data register (RDR).



**Figure 28 Data Read from GRAM through Read Data Register in 18-/16-/9-/8-bit Interface Mode**

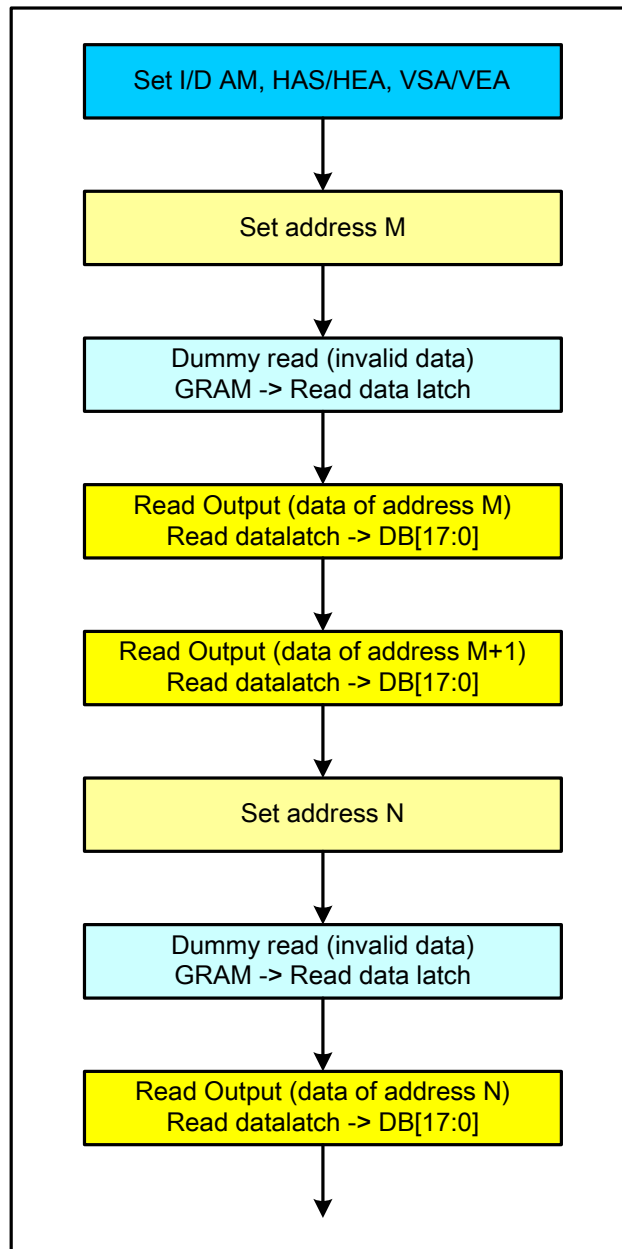


Figure 29 GRAM Data Read Back Flow Chart

### 8.2.22. Power Control 7 (R29h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

**VCM[4:0]** Set the internal VcomH voltage.

VCMR =1, the VcomH voltage is generated based on the VCM[4:0] setting value.

VCMR =0, the VcomH voltage is generated based on the external reference voltage VCOMR.

VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	VREG1OUT x 0.69	1	0	0	0	0	VREG1OUT x 0.85
0	0	0	0	1	VREG1OUT x 0.70	1	0	0	0	1	VREG1OUT x 0.86
0	0	0	1	0	VREG1OUT x 0.71	1	0	0	1	0	VREG1OUT x 0.87
0	0	0	1	1	VREG1OUT x 0.72	1	0	0	1	1	VREG1OUT x 0.88
0	0	1	0	0	VREG1OUT x 0.73	1	0	1	0	0	VREG1OUT x 0.89

0	0	1	0	1	VREG1OUT	x 0.74	1	0	1	0	1	VREG1OUT	x 0.90
0	0	1	1	0	VREG1OUT	x 0.75	1	0	1	1	0	VREG1OUT	x 0.91
0	0	1	1	1	VREG1OUT	x 0.76	1	0	1	1	1	VREG1OUT	x 0.92
0	1	0	0	0	VREG1OUT	x 0.77	1	1	0	0	0	VREG1OUT	x 0.93
0	1	0	0	1	VREG1OUT	x 0.78	1	1	0	0	1	VREG1OUT	x 0.94
0	1	0	1	0	VREG1OUT	x 0.79	1	1	0	1	0	VREG1OUT	x 0.95
0	1	1	1	1	VREG1OUT	x 0.80	1	1	0	1	1	VREG1OUT	x 0.96
0	1	1	0	0	VREG1OUT	x 0.81	1	1	1	0	0	VREG1OUT	x 0.97
0	1	1	0	1	VREG1OUT	x 0.82	1	1	1	0	1	VREG1OUT	x 0.98
0	1	1	1	0	VREG1OUT	x 0.83	1	1	1	1	0	VREG1OUT	x 0.99
0	1	1	1	1	VREG1OUT	x 0.84	1	1	1	1	1	VREG1OUT	x 1.00

### 8.2.23. Frame Rate and Color Control (R2Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	16M_EN	Dither	0	0	0	0	0	0	EXT_R	0	FR_SEL1	FR_SEL0	0	0	0	0

**EXT\_R** External or internal resistor selection for oscillator circuit.

EXT_R	Resistor Selection
0	Internal Resistor (default)
1	External Resistor

**FR\_SEL[1:0]** Set the frame rate when the internal resistor is used for oscillator circuit.

FR_SEL1	FR_SEL0	Frame Rate (Hz)
0	0	90 (default)
0	1	80
1	0	110
1	1	100

**16M\_EN** Select the color depth.

16M_EN	Color Depth Selection
0	262K Color (default)
1	16M Color

**Dither** Dithering function control.

When the dithering function is enabled, the 24-bit input data will be dithered into 18-bit and the display quality is close to 16.7 million colors.

Dither	Dither Function
0	Disable (default)
1	Enable

The input data transfer format is as below (**16M\_EN=1, Dither=1**).

➤ 18bit interface: 2 transfer mode

1<sup>st</sup> Transfer: DB[17:10], DB[8:1]

2<sup>nd</sup> Transfer: DB[17:10]

- 16 bit interface: 2 transfer mode (TRIREG =1, DFM=0)

1<sup>st</sup> Transfer: DB[17:10], DB[8:1]

2<sup>nd</sup> Transfer: DB[17:10]

- 8 bit interface: 3 transfer mode (TRIREG =1, DFM=1)

1<sup>st</sup> Transfer: DB[17:10]

2<sup>nd</sup> Transfer: DB[17:10]

3<sup>rd</sup> Transfer: DB[17:10]

### 8.2.24. Gamma Control (R30h ~ R3Dh)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R30h	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31h	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32h	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35h	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
R36h	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37h	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38h	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39h	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3Ch	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3Dh	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

KP5-0[2:0] :  $\gamma$  fine adjustment register for positive polarity

RP1-0[2:0] :  $\gamma$  gradient adjustment register for positive polarity

VRP1-0[4:0] :  $\gamma$  amplitude adjustment register for positive polarity

KN5-0[2:0] :  $\gamma$  fine adjustment register for negative polarity

RN1-0[2:0] :  $\gamma$  gradient adjustment register for negative polarity

VRN1-0[4:0] :  $\gamma$  amplitude adjustment register for negative polarity

For details “ $\gamma$ -Correction Function” section.

### 8.2.25. Horizontal and Vertical RAM Address Position (R50h, R51h, R52h, R53h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R51h	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
R52h	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R53h	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0

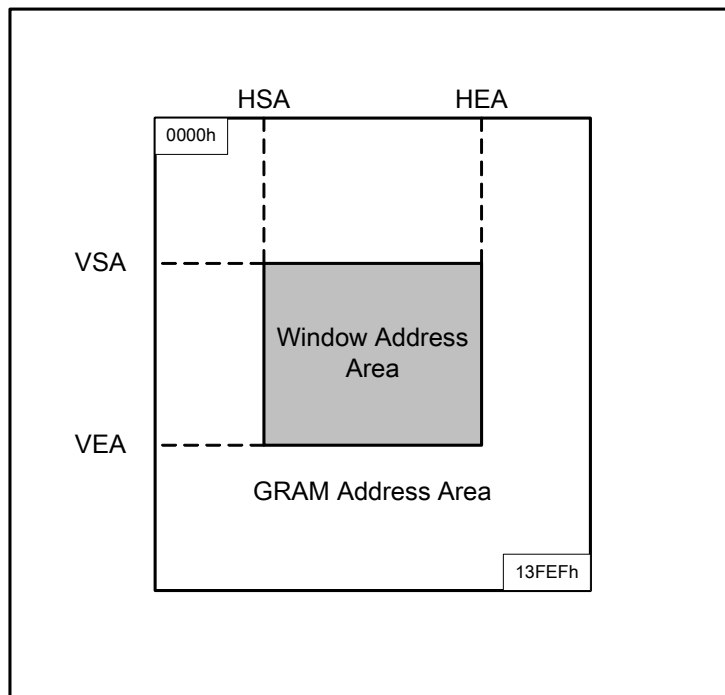
**HSA[7:0]/HEA[7:0]** HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the

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window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure “00”h ≤ HSA[7:0] < HEA[7:0] ≤ “EF”h. and “04”h ≤ HEA-HAS.

**VSA[8:0]/VEA[8:0]** VSA[8:0] and VEA[8:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure “000”h ≤ VSA[8:0] < VEA[8:0] ≤ “13F”h.



**Figure 30 GRAM Access Range Configuration**

$$“00”h \leq HAS[7:0] \leq HEA[7:0] \leq “EF”h$$

$$“00”h \leq VSA[7:0] \leq VEA[7:0] \leq “13F”h$$

Note1. The window address range must be within the GRAM address space.

Note2. Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

**8.2.26. Gate Scan Control (R60h, R61h, R6Ah)**

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R60h	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R61h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
R6Ah	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

**SCN[5:0]** The ILI9320 allows to specify the gate line from which the gate driver starts to scan by setting the

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SCN[5:0] bits.

SCN[5:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h	G1	G320	G1	G320
01h	G9	G312	G17	G304
02h	G17	G304	G33	G288
03h	G25	G296	G49	G272
04h	G33	G288	G65	G256
05h	G41	G280	G81	G240
06h	G49	G272	G97	G224
07h	G57	G264	G113	G208
08h	G65	G256	G129	G192
09h	G73	G248	G145	G176
0Ah	G81	G240	G161	G160
0Bh	G89	G232	G177	G144
0Ch	G97	G224	G193	G128
0Dh	G105	G216	G209	G112
0Eh	G113	G208	G2	G96
0Fh	G121	G200	G18	G80
10h	G129	G192	G34	G64
11h	G137	G184	G50	G48
12h	G145	G176	G66	G32
13h	G153	G168	G82	G16
14h	G161	G160	G98	G319
15h	G169	G152	G114	G303
16h	G177	G144	G130	G287
17h	G185	G136	G146	G271
18h	G193	G128	G162	G255
19h	G201	G120	G178	G239
1Ah	G209	G112	G194	G223
1Bh	G217	G104	G114	G207
1Ch	G225	G96	G130	G191
1Dh	G233	G88	G146	G175
1Eh	G241	G80	G162	G159
1Fh	G249	G72	G178	G143
20h	G257	G64	G194	G127
21h	G265	G56	G210	G111
22h	G273	G48	G226	G95
23h	G281	G40	G242	G79
24h	G289	G32	G258	G63
25h	G297	G24	G274	G47
26h	G305	G16	G290	G31
27h	G313	G8	G306	G15
28h ~ 3Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled

**NL[5:0]:** Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

**NL[5:0]      LCD Drive Line**

6'h1D	240 lines
6'h1E	248 lines
6'h1F	256 lines
6'h20	264 lines
6'h21	272 lines
6'h22	280 lines
6'h23	288 lines
6'h24	296 lines
6'h25	304 lines
6'h26	312 line
6'h27	320 line
Others	Setting inhibited

**NDL:** Sets the source driver output level in the non-display area.

NDL	Non-Display Area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

**GS:** Sets the direction of scan by the gate driver in the range determined by SCN[4:0] and NL[4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G320.

When GS = 1, the scan direction is from G320 to G1

**REV:** Enables the grayscale inversion of the image by setting REV=1.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	negative polarity
0	18'h00000	V63	V0
	·	·	·
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	·	·	·
	18'h3FFFF	V63	V0

**VLE:** Vertical scroll display enable bit. When VLE = 1, the ILI9320 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image Display
0	Fixed

1	Enable Scrolling
---	------------------

**VL[8:0]:** Sets the scrolling amount of base image. The base image is scrolled in vertical direction and displayed from the line determined by VL[8:0]. Make sure that VL[8:0] ≤ 320.

### 8.2.27. Partial Image 1 Display Position (R80h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTD P0[8]	PTD P0[7]	PTD P0[6]	PTD P0[5]	PTD P0[4]	PTD P0[3]	PTD P0[2]	PTD P0[1]	PTD P0[0]

**PTDP0[8:0]:** Sets the display position of partial image 1. The display areas of the partial images 1 and 2 must not overlap each another.

### 8.2.28. Partial Image 1 RAM Start/End Address (R81h, R82h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTS A0[8]	PTS A0[7]	PTS A0[6]	PTS A0[5]	PTS A0[4]	PTS A0[3]	PTS A0[2]	PTS A0[1]	PTS A0[0]
W	1	0	0	0	0	0	0	0	PTE A0[8]	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]

**PTSA0[8:0] PTEA0[8:0]:** Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[8:0] ≤ PTEA0[8:0].

### 8.2.29. Partial Image 2 Display Position (R83h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTS A1[8]	PTD P1[7]	PTD P1[6]	PTD P1[5]	PTD P1[4]	PTD P1[3]	PTD P1[2]	PTD P1[1]	PTD P1[0]

**PTDP1[8:0]:** Sets the display position of partial image 2. The display areas of the partial images 1 and 2 must not overlap each another.

### 8.2.30. Partial Image 2 RAM Start/End Address (R84h, R85h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTS A1[8]	PTS A1[7]	PTS A1[6]	PTS A1[5]	PTS A1[4]	PTS A1[3]	PTS A1[2]	PTS A1[1]	PTS A1[0]
W	1	0	0	0	0	0	0	0	PTE A1[8]	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]

**PTSA1[8:0] PTEA1[8:0]:** Sets the start line address and the end line address of the RAM area storing the data of partial image 2. Make sure PTSA1[8:0] ≤ PTEA1[8:0].

### 8.2.31. Panel Interface Control 1 (R90h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----	----	-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----

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W	1	0	0	0	0	0	0	0	DIV11	DIV10	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
---	---	---	---	---	---	---	---	---	-------	-------	---	---	-------	-------	-------	-------	-------

**RTNI[4:0]:** Sets 1H (line) clock number of internal clock operating mode. In this mode, ILI9320 display operation is synchronized with internal clock signal.

RTNI[4:0]	Clocks/Line	RTNI[4:0]	Clocks/Line
00000~01111	Setting Disabled	11000	24 clocks
10000	16 clocks	11001	25 clocks
10001	17 clocks	11010	26 clocks
10010	18 clocks	11011	27 clocks
10011	19 clocks	11100	28 clocks
10100	20 clocks	11101	29 clocks
10101	21 clocks	11110	30 clocks
10110	22 clocks	11111	31 clocks
10111	23 clocks		

**DIVI[1:0]:** Sets the division ratio of internal clock frequency.

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	f <sub>osc</sub> / 1
0	1	2	f <sub>osc</sub> / 2
1	0	4	f <sub>osc</sub> / 4
1	1	8	f <sub>osc</sub> / 8

Formula to calculate frame frequency

$$\text{Frame Rate} = \frac{f_{osc}}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Lines} + \text{BP} + \text{FP})}$$

- f<sub>osc</sub> : frequency if RC oscillation.
- Clock cycles per line : RTN bits
- Division ratio : DIV bits
- Lines : number of lines for driving the LCD panel.
- FP: Front porch lines
- BP; Back porch lines

### 8.2.32. Panel Interface Control 2 (R92h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0

**NOWI[2:0]:** Sets the gate output non-overlap period when ILI9320 display operation is synchronized with internal clock signal.

NOWI[2:0]	Gate Non-overlap Period
000	0 clocks
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	7 clocks

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

### 8.2.33. Panel Interface Control 3 (R93h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI2	MCPI1	MCPI0

**MCPI[2:0]:** Sets the source output position when ILI9320 display operation is synchronized with internal clock signal.

MCPI[2:0]	Source Output Position
000	Setting inhibited
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	7 clocks

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI[1:0]), from the reference point.

### 8.2.34. Panel Interface Control 4 (R95h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0

**RTNE[5:0]:** Sets 1H (line) clock number of RGB interface mode. In this mode, ILI9320 display operation is synchronized with RGB interface signals.

$$DIVE \text{ (division ratio)} \times RTNE \text{ (DOTCLKs)} \leq \text{DOTCLKs in 1H period.}$$

RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)
00h	Setting Prohibited	10h	16 clocks	20h	32 clocks	30h	48 clocks
01h	Setting Prohibited	11h	17 clocks	21h	33 clocks	31h	49 clocks
02h	Setting Prohibited	12h	18 clocks	22h	34 clocks	32h	50 clocks
03h	Setting Prohibited	13h	19 clocks	23h	35 clocks	33h	51 clocks
04h	Setting Prohibited	14h	20 clocks	24h	36 clocks	34h	52 clocks
05h	Setting Prohibited	15h	21 clocks	25h	37 clocks	35h	53 clocks
06h	Setting Prohibited	16h	22 clocks	26h	38 clocks	36h	54 clocks
07h	Setting Prohibited	17h	23 clocks	27h	39 clocks	37h	55 clocks
08h	Setting Prohibited	18h	24 clocks	28h	40 clocks	38h	56 clocks
09h	Setting Prohibited	19h	25 clocks	29h	41 clocks	39h	57 clocks
0ah	Setting Prohibited	1ah	26 clocks	2ah	42 clocks	3ah	58 clocks
0bh	Setting Prohibited	1bh	27 clocks	2bh	43 clocks	3bh	59 clocks
0ch	Setting Prohibited	1ch	28 clocks	2ch	44 clocks	3ch	60 clocks
0dh	Setting Prohibited	1dh	29 clocks	2dh	45 clocks	3dh	61 clocks
0eh	Setting Prohibited	1eh	30 clocks	2eh	46 clocks	3eh	62 clocks
0fh	Setting Prohibited	1fh	31 clocks	2fh	47 clocks	3fh	63 clocks

**DIVE[1:0]:** Sets the division ratio of DOTCLK when ILI9320 display operation is synchronized with RGB interface signals.

DIVE[1:0]	Division Ratio	18/16-bit RGB Interface	DOTCLK=5MHz	6-bit x 3 Transfers RGB Interface	DOTCLK=5MHz
00	Setting Prohibited	Setting Prohibited	-	Setting Prohibited	-
01	1/4	4 DOTCLKS	0.8 $\mu$ s	12 DOTCLKS	0.8 $\mu$ s
10	1/8	8 DOTCLKS	1.6 $\mu$ s	24 DOTCLKS	1.6 $\mu$ s
11	1/16	16 DOTCLKS	3.2 $\mu$ s	48 DOTCLKS	3.2 $\mu$ s

### 8.2.35. Panel Interface Control 5 (R97h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0

**NOWE[2:0]:** Sets the gate output non-overlap period when the ILI9320 display operation is synchronized with RGB interface signals.

NOWE[3:0]	Gate Non-overlap Period	NOWE[3:0]	Gate Non-overlap Period
0000	0 clocks	1000	8 clocks
0001	1 clocks	1001	9 clocks
0010	2 clocks	1010	10 clocks
0011	3 clocks	1011	11 clocks
0100	4 clocks	1100	12 clocks
0101	5 clocks	1101	13 clocks
0110	6 clocks	1110	14 clocks
0111	7 clocks	1111	15 clocks

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

### 8.2.36. Panel Interface Control 6 (R98h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2	MCPE1	MCPE0

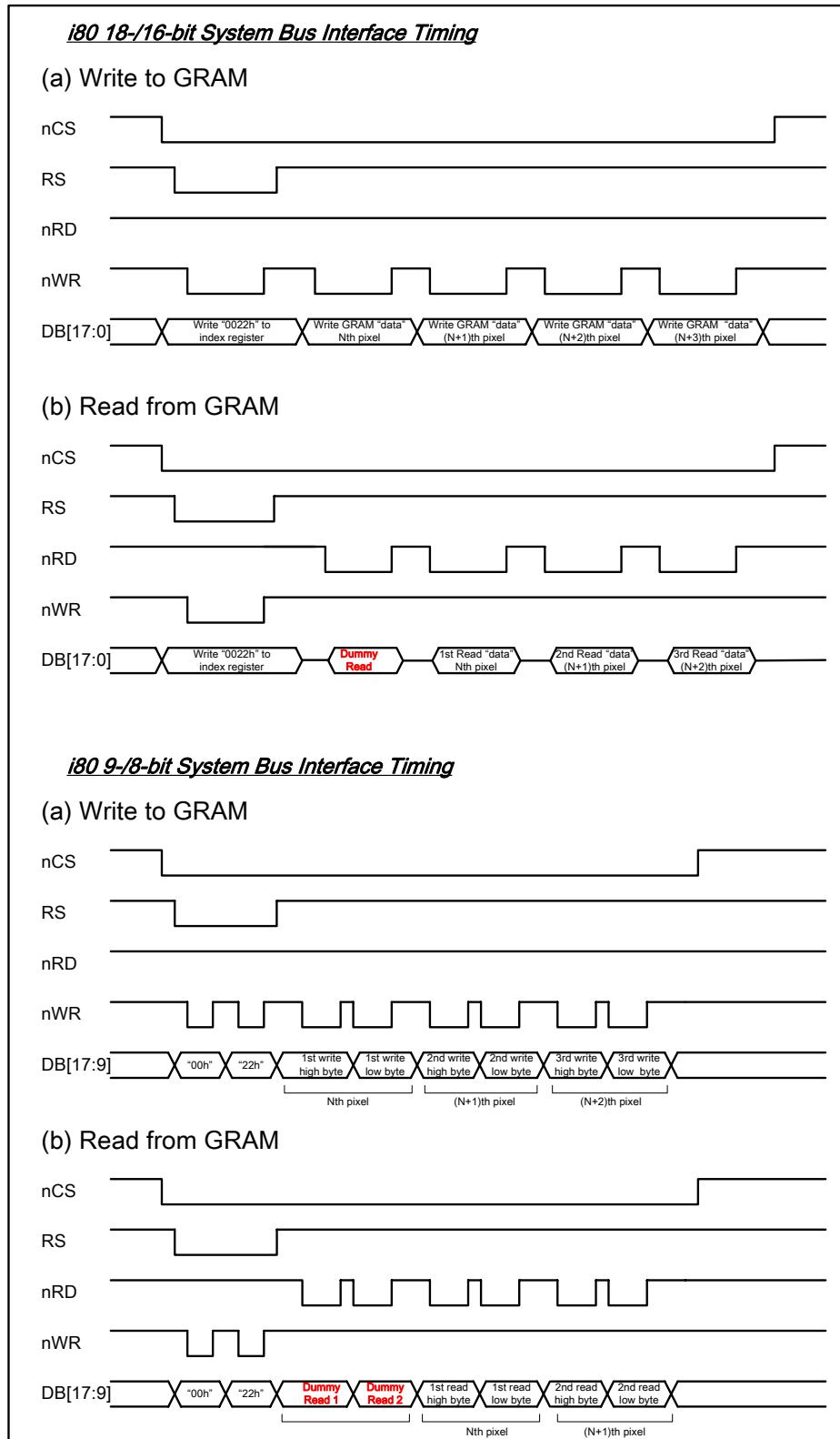
**MCPE[2:0]:** Sets the source output position when the ILI9320 display operation is synchronized with RGB interface signals.

MCPE[2:0]	Source Output Position
000	0 clocks
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	7 clocks

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

## 9. GRAM Address Map & Read/Write

ILI9320 has an internal graphics RAM (GRAM) of 87,120 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80 system, SPI and RGB interfaces.



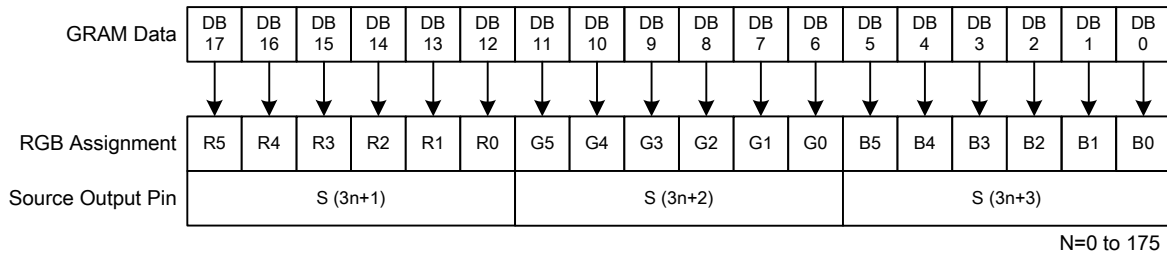
**Figure31 GRAM Read/Write Timing of i80-System Interface**



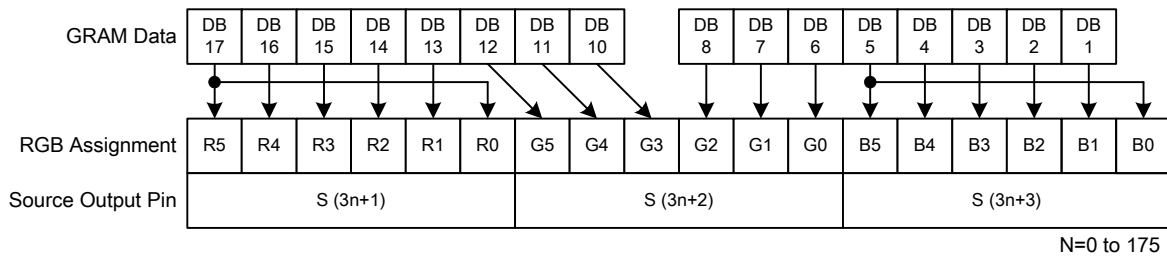
GRAM address map table of SS=0, BGR=0

SS=0, BGR=0		S1...S3	S4...S6	S7...S9	S10...S12	...	S517...S519	S520...S522	S523...S525	S526...S720
GS=0	GS=1	DB17...0	DB17...0	DB17...0	DB17...0	...	DB17...0	DB17...0	DB17...0	DB17...0
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	...	"000ECh"	"000EDh"	"000EEh"	"000EFh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	...	"001ECh"	"001EDh"	"001EEh"	"001EFh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	...	"002ECh"	"002EDh"	"002EEh"	"002EFh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	...	"003ECh"	"003EDh"	"003EEh"	"003EFh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	...	"004ECh"	"004EDh"	"004EEh"	"004EFh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	...	"005ECh"	"005EDh"	"005EEh"	"005EFh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	...	"006ECh"	"006EDh"	"006EEh"	"006EFh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	...	"007ECh"	"007EDh"	"007EEh"	"007EFh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	...	"008ECh"	"008EDh"	"008EEh"	"008EFh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	...	"009ECh"	"009EDh"	"009EEh"	"009EFh"
.	.	.	.	.	.	...	.	.	.	.
.	.	.	.	.	.	...	.	.	.	.
.	.	.	.	.	.	...	.	.	.	.
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	...	"136ECh"	"136EDh"	"136EEh"	"136EFh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	...	"137ECh"	"137EDh"	"137EEh"	"137EFh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	...	"138ECh"	"138EDh"	"138EEh"	"138EFh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	...	"139ECh"	"139EDh"	"139EEh"	"139EFh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	...	"13AECh"	"13AEDh"	"13AEEh"	"13AEFh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	...	"13BECh"	"13BEDh"	"13BEEh"	"13BEFh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	...	"13CECh"	"13CEDh"	"13CEEh"	"13CEFh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	...	"13DECh"	"13DEDh"	"13DEEh"	"13DEFh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	...	"13EECh"	"13EEDh"	"13EEEh"	"13EEFh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	...	"13FECh"	"13FEDh"	"13FEEh"	"13FEFh"

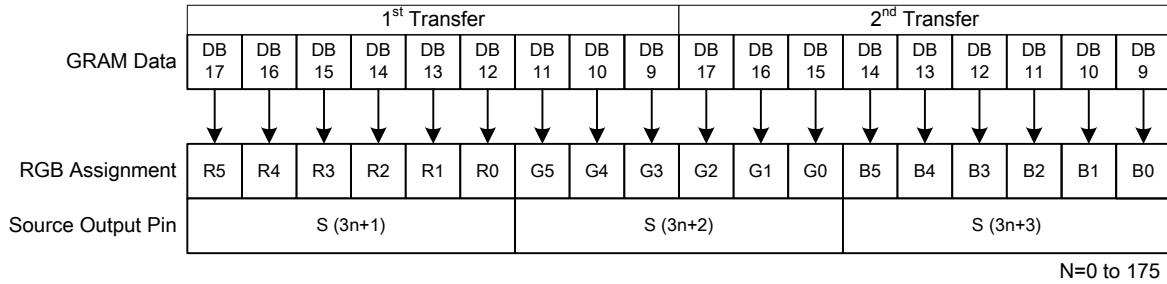
***i80/M68 system 18-bit data bus interface***



***i80/M68 system 16-bit data bus interface***



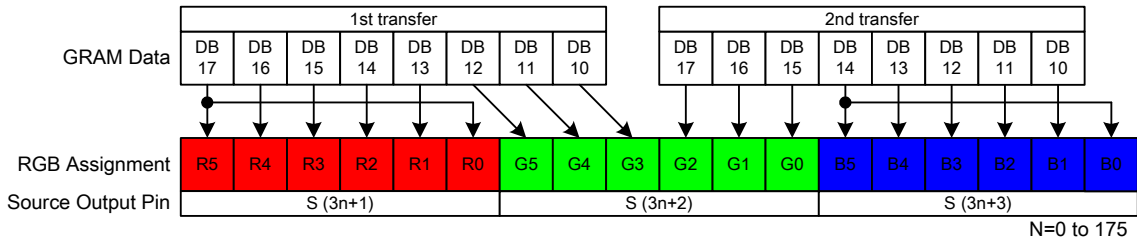
***i80/M68 system 9-bit data bus interface***



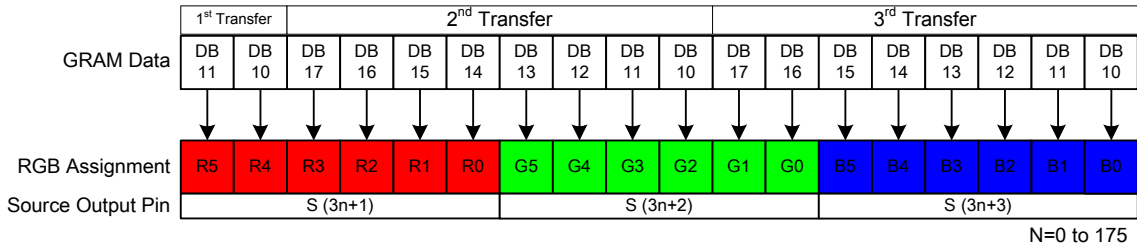
GRAM Data and display data of 18-/16-/9-bit system interface (SS="0", BGR="0")

**Figure32 i80-System Interface with 18-/16-/9-bit Data Bus (SS="0", BGR="0")**

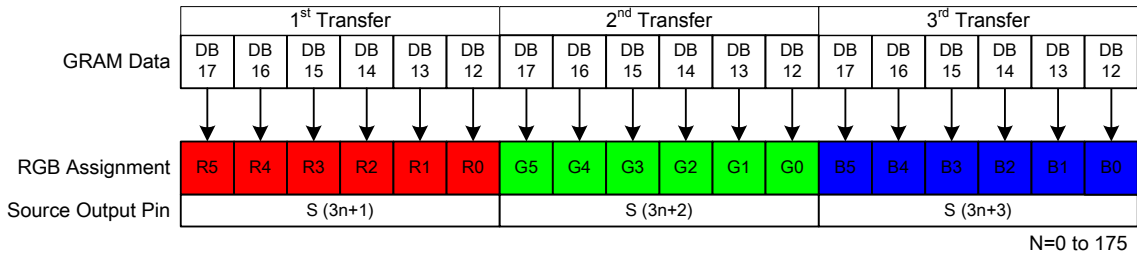
*i80/M68 system 8-bit interface / SPI Interface (2 transfers/pixel)*



*i80/M68 system 8-bit interface (3 transfers/pixel, TRI="1", DFM[1:0]="00")*



*i80/M68 system 8-bit interface (3 transfers/pixel, TRI="1", DFM[1:0]="10")*



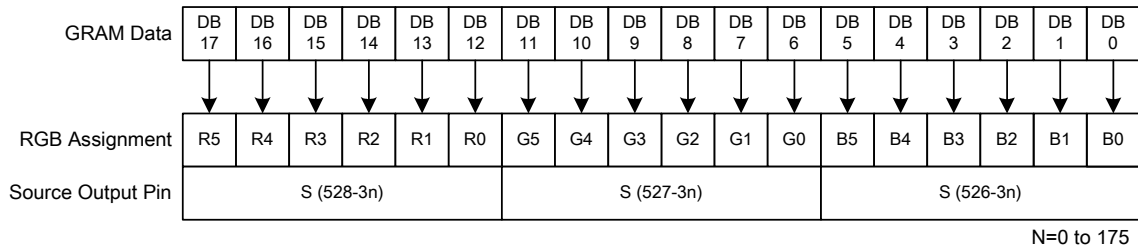
*i80/M68 system 8-bit interface (SS="0", BGR="0")*

**Figure33 i80-System Interface with 8-bit Data Bus (SS="0", BGR="0")**

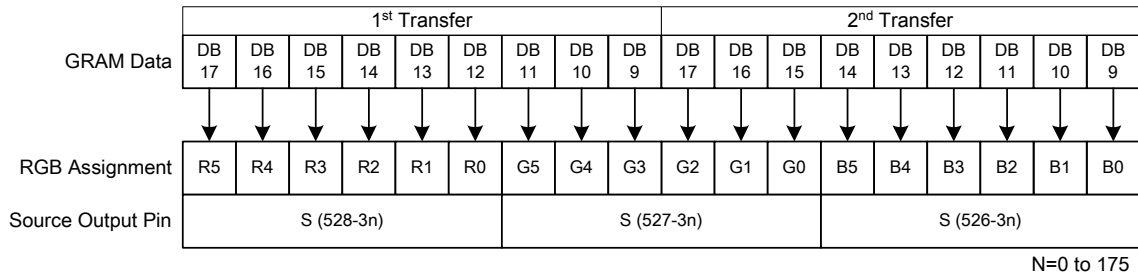
GRAM address map table of SS=1, BGR=1

SS=0, BGR=0	S720...S718	S717...S715	S714...S712	S711...S709	...	S12...S10	S9...S7	S6...S4	S3...S1	
GS=0	GS=1	DB17...0	DB17...0	DB17...0	DB17...0	...	DB17...0	DB17...0	DB17...0	DB17...0
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	...	"000ECh"	"000EDh"	"000EEh"	"000EFh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	...	"001ECh"	"001EDh"	"001EEh"	"001EFh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	...	"002ECh"	"002EDh"	"002EEh"	"002EFh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	...	"003ECh"	"003EDh"	"003EEh"	"003EFh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	...	"004ECh"	"004EDh"	"004EEh"	"004EFh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	...	"005ECh"	"005EDh"	"005EEh"	"005EFh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	...	"006ECh"	"006EDh"	"006EEh"	"006EFh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	...	"007ECh"	"007EDh"	"007EEh"	"007EFh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	...	"008ECh"	"008EDh"	"008EEh"	"008EFh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	...	"009ECh"	"009EDh"	"009EEh"	"009EFh"
.	.	.	.	.	.	...	.	.	.	.
.	.	.	.	.	.	...	.	.	.	.
.	.	.	.	.	.	...	.	.	.	.
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	...	"136ECh"	"136EDh"	"136EEh"	"136EFh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	...	"137ECh"	"137EDh"	"137EEh"	"137EFh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	...	"138ECh"	"138EDh"	"138EEh"	"138EFh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	...	"139ECh"	"139EDh"	"139EEh"	"139EFh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	...	"13AECh"	"13AEDh"	"13AEEh"	"13AEFh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	...	"13BECh"	"13BEDh"	"13BEEh"	"13BEFh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	...	"13CECh"	"13CEDh"	"13CEEh"	"13CEFh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	...	"13DECh"	"13DEDh"	"13DEEh"	"13DEFh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	...	"13EECh"	"13EEDh"	"13EEEh"	"13EEFh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	...	"13FECh"	"13FEDh"	"13FEEh"	"13FEFh"

***i80/M68 system 18-bit data bus interface***



***i80/M68 system 9-bit data bus interface***



GRAM Data and display data of 18-/9-bit system interface (SS="1", BGR="1")

**Figure 34 i80-System Interface with 18-/9-bit Data Bus (SS="1", BGR="1")**

## 10. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[8:0], end: VEA[8:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the ILI9320 to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the GRAM address bits (RAM address set register) must be an address within the window address area.

[Window address setting area]

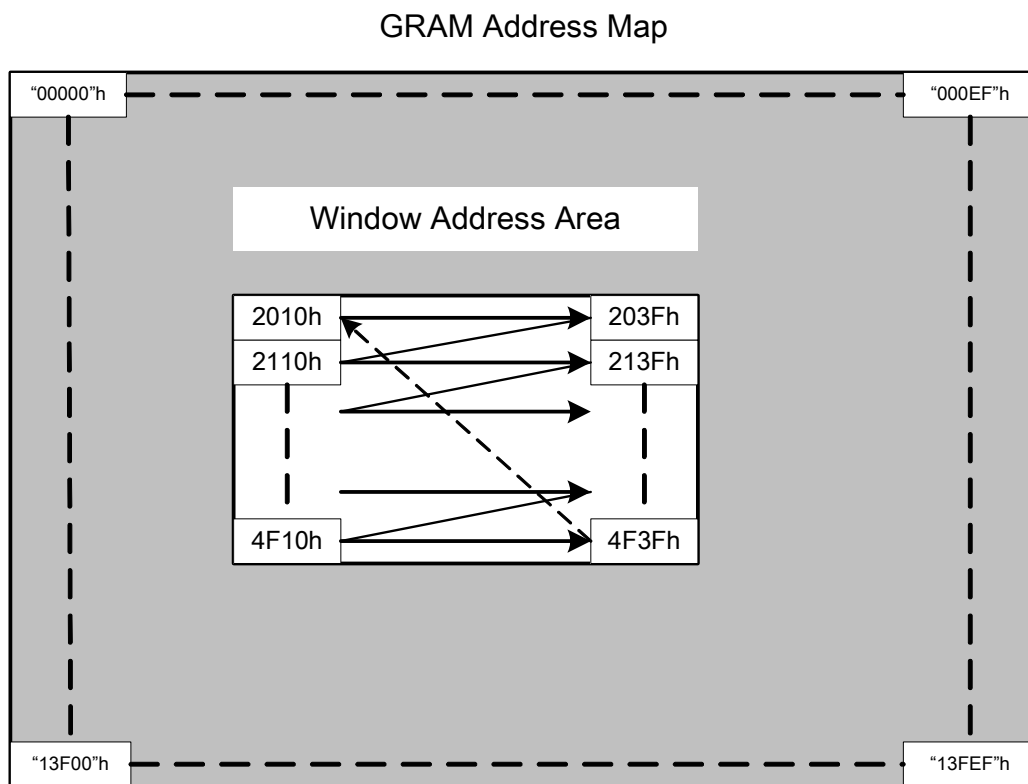
(Horizontal direction)  $00H \leq HSA[7:0] \leq HEA[7:0] \leq "EF"H$

(Vertical direction)  $00H \leq VSA[8:0] \leq VEA[8:0] \leq "13F"H$

[RAM address, AD (an address within a window address area)]

(RAM address)  $HSA[7:0] \leq AD[7:0] \leq HEA[7:0]$

$VSA[8:0] \leq AD[15:8] \leq VEA[8:0]$



Window address setting area

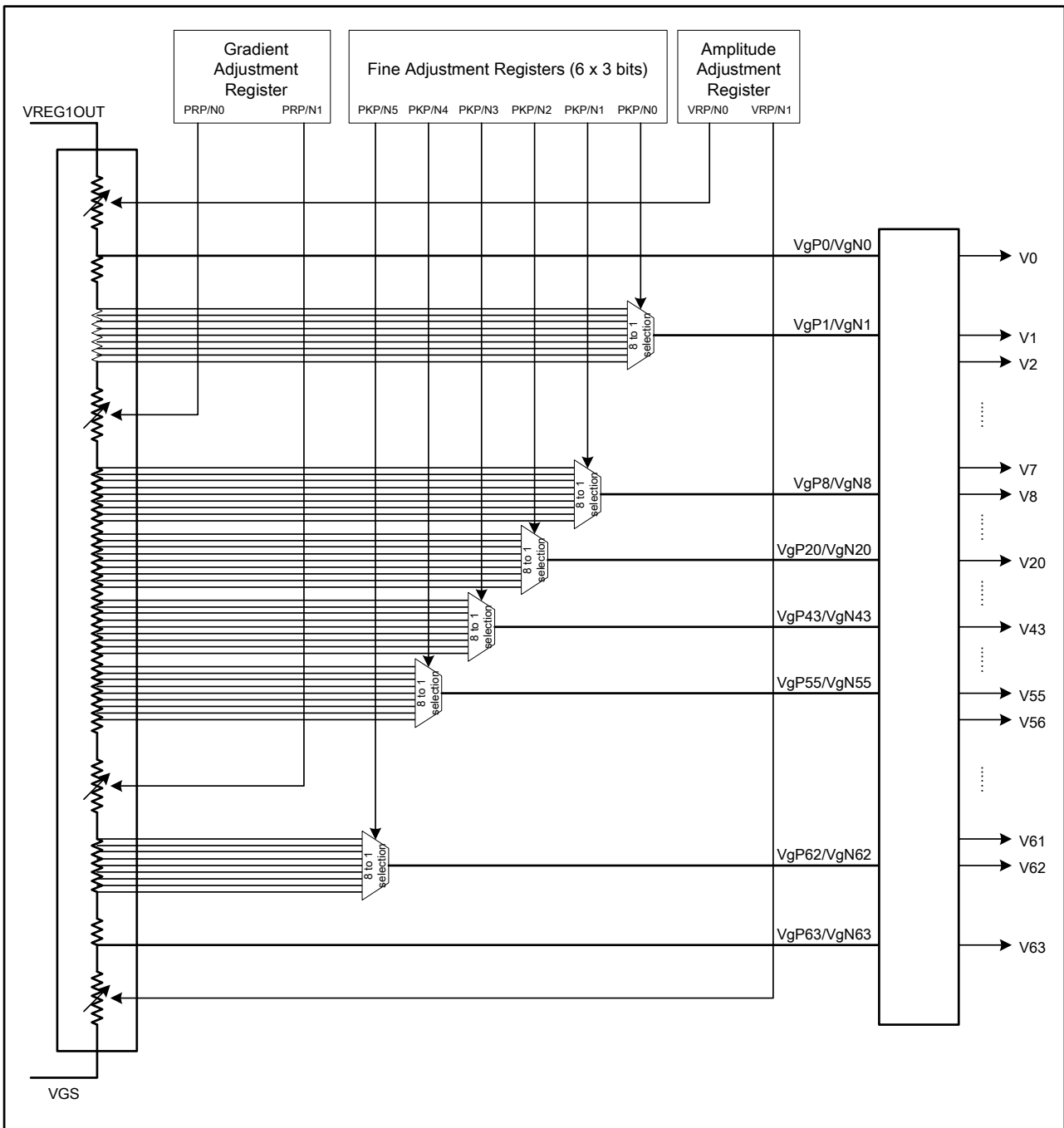
HSA[7:0] = 10h, HSA[7:0] = 3Fh, I/D = 1 (increment)  
VSA[8:0] = 20h, VSA[8:0] = 4Fh, AM = 0 (horizontal writing)

**Figure 35 GRAM Access Window Map**



## 11. Gamma Correction

ILI9320 incorporates the  $\gamma$ -correction function to display 262,144 colors for the LCD panel. The  $\gamma$ -correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9320 available with liquid crystal panels of various characteristics.



**Figure 36 Grayscale Voltage Generation**



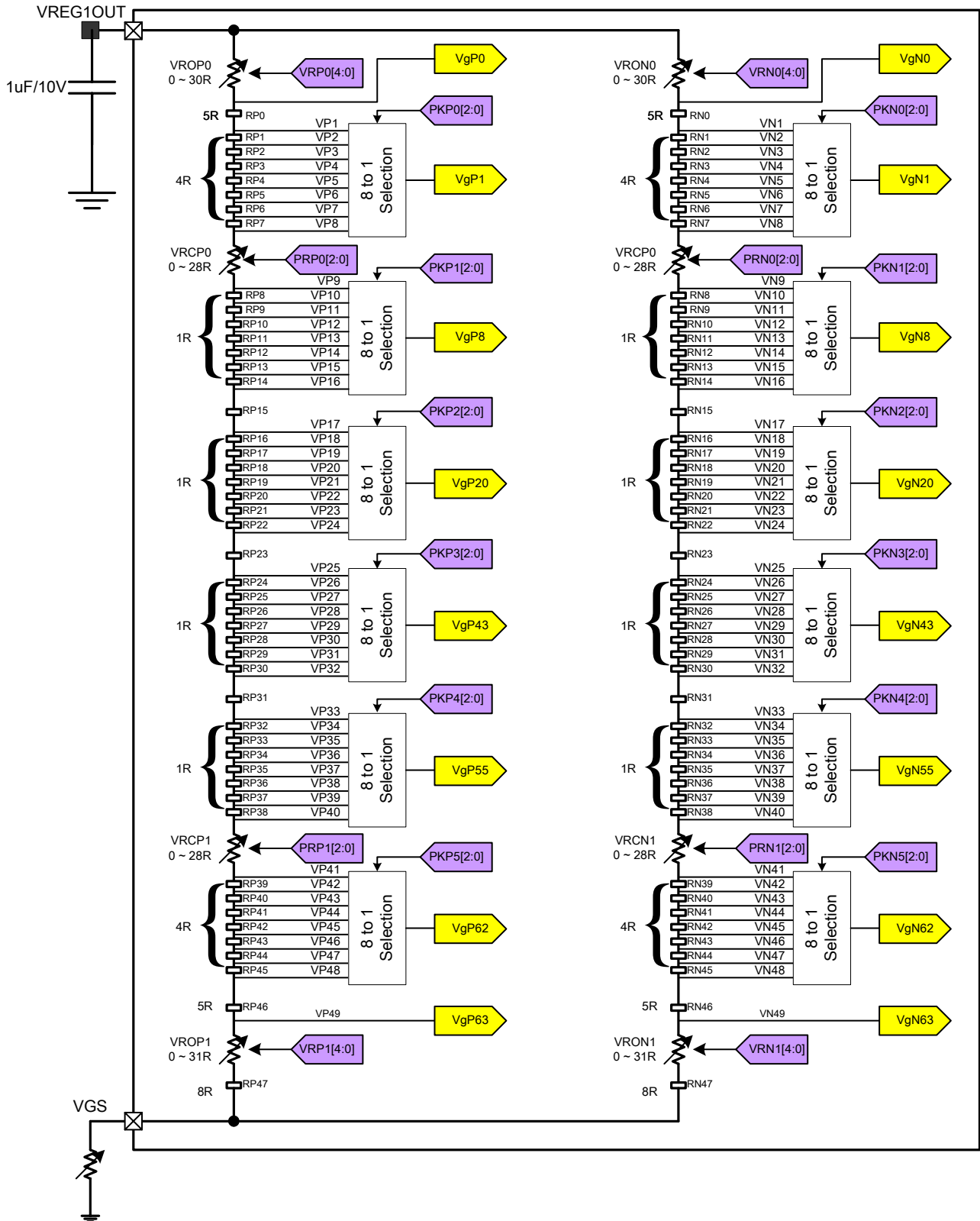


Figure 37 Grayscale Voltage Adjustment

1. Gradient adjustment registers

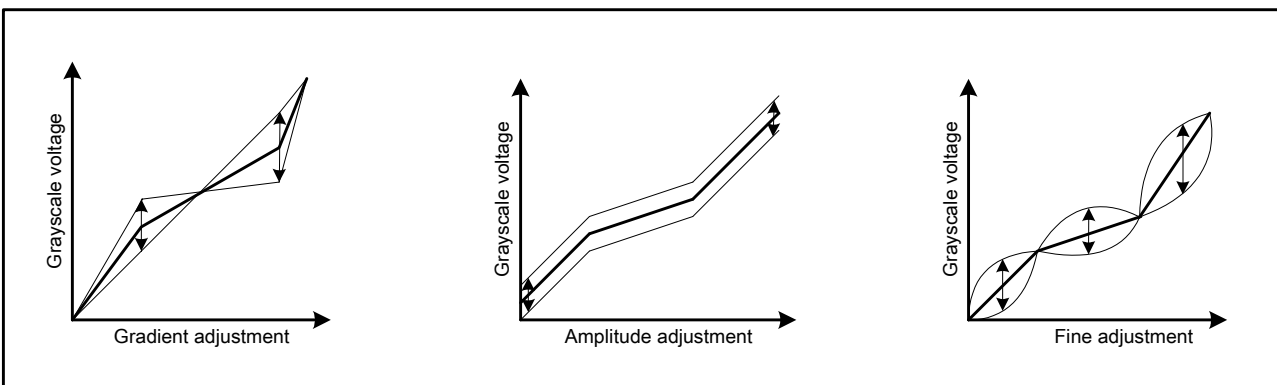
The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[4:0]/VRN0[4:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.



**Figure 38 Gamma Curve Adjustment**

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRCP0, VRCN0
	PRP1 [2:0]	PRN1 [2:0]	Variable resistor VRCP1, VRCN1
Amplitude adjustment	VRP0 [4:0]	VRN0 [4:0]	Variable resistor VROP0, VRON0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0 [2:0]	KN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	KP1 [2:0]	KN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	KP2 [2:0]	KN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	KP3 [2:0]	KN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	KP4 [2:0]	KN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	KP5 [2:0]	KN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

### Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the  $\gamma$ -correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

### Variable resistors

ILI9320 uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment		Amplitude adjustment (1)		Amplitude adjustment (2)	
PRP(N)0/1[2:0]	VRCP(N)0	VRP(N)0[4:0]	VROP(N)0	VRP(N)1[4:0]	VROP(N)1
Register	Resistance	Register	Resistance	Register	Resistance
000	0R	0000	0R	00000	0R
001	4R	0001	2R	00001	1R
010	8R	0010	4R	00010	2R
011	12R	:	:	:	:
100	16R	:	:	:	:
101	20R	1101	26R	11101	29R
110	24R	1111	28R	11110	30R
111	28R	1111	30R	11111	31R

### 8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine adjustment registers and selected voltage						
Register	Selected Voltage					
KP(N)[2:0]	VgP(N)1	VgP(N)8	VgP(N)20	VgP(N)43	VgP(N)55	VgP(N)62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formulae.

Formulae for calculating voltage (Positive polarity)

Reference Voltage	Fine Adjustment Value	Formula	Vout
VgP0	—	$VREG1OUT - VD * VROP0 / sumRP$	VP0
VgP1	KP0[2:0]=000	$VREG1OUT - VD * (VROP0 + 5R) / sumRP$	VP1
	KP0[2:0]=001	$VREG1OUT - VD * (VROP0 + 9R) / sumRP$	VP2
	KP0[2:0]=010	$VREG1OUT - VD * (VROP0 + 13R) / sumRP$	VP3
	KP0[2:0]=011	$VREG1OUT - VD * (VROP0 + 17R) / sumRP$	VP4
	KP0[2:0]=100	$VREG1OUT - VD * (VROP0 + 21R) / sumRP$	VP5
	KP0[2:0]=101	$VREG1OUT - VD * (VROP0 + 25R) / sumRP$	VP6
	KP0[2:0]=110	$VREG1OUT - VD * (VROP0 + 29R) / sumRP$	VP7
	KP0[2:0]=111	$VREG1OUT - VD * (VROP0 + 33R) / sumRP$	VP8
VgP8	KP1[2:0]=000	$VREG1OUT - VD * (VROP0 + 33R + VRCP0) / sumRP$	VP9
	KP1[2:0]=001	$VREG1OUT - VD * (VROP0 + 34R + VRCP0) / sumRP$	VP10
	KP1[2:0]=010	$VREG1OUT - VD * (VROP0 + 35R + VRCP0) / sumRP$	VP11
	KP1[2:0]=011	$VREG1OUT - VD * (VROP0 + 36R + VRCP0) / sumRP$	VP12
	KP1[2:0]=100	$VREG1OUT - VD * (VROP0 + 37R + VRCP0) / sumRP$	VP13
	KP1[2:0]=101	$VREG1OUT - VD * (VROP0 + 38R + VRCP0) / sumRP$	VP14
	KP1[2:0]=110	$VREG1OUT - VD * (VROP0 + 39R + VRCP0) / sumRP$	VP15
	KP1[2:0]=111	$VREG1OUT - VD * (VROP0 + 40R + VRCP0) / sumRP$	VP16
VgP20	KP2[2:0]=000	$VREG1OUT - VD * (VROP0 + 45R + VRCP0) / sumRP$	VP17
	KP2[2:0]=001	$VREG1OUT - VD * (VROP0 + 46R + VRCP0) / sumRP$	VP18
	KP2[2:0]=010	$VREG1OUT - VD * (VROP0 + 47R + VRCP0) / sumRP$	VP19
	KP2[2:0]=011	$VREG1OUT - VD * (VROP0 + 48R + VRCP0) / sumRP$	VP20
	KP2[2:0]=100	$VREG1OUT - VD * (VROP0 + 49R + VRCP0) / sumRP$	VP21
	KP2[2:0]=101	$VREG1OUT - VD * (VROP0 + 50R + VRCP0) / sumRP$	VP22
	KP2[2:0]=110	$VREG1OUT - VD * (VROP0 + 51R + VRCP0) / sumRP$	VP23
	KP2[2:0]=111	$VREG1OUT - VD * (VROP0 + 52R + VRCP0) / sumRP$	VP24
VgP43	KP3[2:0]=000	$VREG1OUT - VD * (VROP0 + 68R + VRCP0) / sumRP$	VP25
	KP3[2:0]=001	$VREG1OUT - VD * (VROP0 + 69R + VRCP0) / sumRP$	VP26
	KP3[2:0]=010	$VREG1OUT - VD * (VROP0 + 70R + VRCP0) / sumRP$	VP27
	KP3[2:0]=011	$VREG1OUT - VD * (VROP0 + 71R + VRCP0) / sumRP$	VP28
	KP3[2:0]=100	$VREG1OUT - VD * (VROP0 + 72R + VRCP0) / sumRP$	VP29
	KP3[2:0]=101	$VREG1OUT - VD * (VROP0 + 73R + VRCP0) / sumRP$	VP30
	KP3[2:0]=110	$VREG1OUT - VD * (VROP0 + 74R + VRCP0) / sumRP$	VP31
	KP3[2:0]=111	$VREG1OUT - VD * (VROP0 + 75R + VRCP0) / sumRP$	VP32
VgP55	KP4[2:0]=000	$VREG1OUT - VD * (VROP0 + 80R + VRCP0) / sumRP$	VP33
	KP4[2:0]=001	$VREG1OUT - VD * (VROP0 + 81R + VRCP0) / sumRP$	VP34
	KP4[2:0]=010	$VREG1OUT - VD * (VROP0 + 82R + VRCP0) / sumRP$	VP35
	KP4[2:0]=011	$VREG1OUT - VD * (VROP0 + 83R + VRCP0) / sumRP$	VP36
	KP4[2:0]=100	$VREG1OUT - VD * (VROP0 + 84R + VRCP0) / sumRP$	VP37
	KP4[2:0]=101	$VREG1OUT - VD * (VROP0 + 85R + VRCP0) / sumRP$	VP38
	KP4[2:0]=110	$VREG1OUT - VD * (VROP0 + 86R + VRCP0) / sumRP$	VP39
	KP4[2:0]=111	$VREG1OUT - VD * (VROP0 + 87R + VRCP0) / sumRP$	VP40
VgP62	KP5[2:0]=000	$VREG1OUT - VD * (VROP0 + 87R + VRCP0 + VRCP1) / sumRP$	VP41
	KP5[2:0]=001	$VREG1OUT - VD * (VROP0 + 91R + VRCP0 + VRCP1) / sumRP$	VP42
	KP5[2:0]=010	$VREG1OUT - VD * (VROP0 + 95R + VRCP0 + VRCP1) / sumRP$	VP43
	KP5[2:0]=011	$VREG1OUT - VD * (VROP0 + 99R + VRCP0 + VRCP1) / sumRP$	VP44
	KP5[2:0]=100	$VREG1OUT - VD * (VROP0 + 103R + VRCP0 + VRCP1) / sumRP$	VP45
	KP5[2:0]=101	$VREG1OUT - VD * (VROP0 + 107R + VRCP0 + VRCP1) / sumRP$	VP46
	KP5[2:0]=110	$VREG1OUT - VD * (VROP0 + 111R + VRCP0 + VRCP1) / sumRP$	VP47
	KP5[2:0]=111	$VREG1OUT - VD * (VROP0 + 115R + VRCP0 + VRCP1) / sumRP$	VP48

VgP63	—	VREG1OUT -VD*(VROP0+120R+VRCP0+VRCP1)/sumRP	VP49
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Sum of positive resistor sumRP = 128R + VROP0 + VROP1 + VRCP0 + VRCP1

Sum of negative resistor sumRN = 128R + VRON0 + VRON1 + VRCN0 + VRCN1

Voltage difference VD = (VREG1OUT – VGS)

**Formulae for calculating voltage (Positive polarity)**

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VgP0	V32	V43+(V20-V43)*(11/23)
V1	VgP1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VgP8	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VgP43
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VgP20	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VgP55
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VgP62
V31	V43+(V20-V43)*(12/23)	V63	VgP63

Note: The following condition shall be always retained.

DDVDH – V0 > 0.5V

DDVDH – V8 > 1.1V

V55 – AGND > 1.1V

**Formulae for calculating voltage (Negative polarity)**

Reference Voltage	Fine Adjustment Value	Formula	Vout
VgN0	—	$VREG1OUT - VD * VRON0 / sumRN$	VN0
VgN1	KN0[2:0]=000	$VREG1OUT - VD * (VRON0 + 5R) / sumRN$	VN1
	KN0[2:0]=001	$VREG1OUT - VD * (VRON0 + 9R) / sumRN$	VN2
	KN0[2:0]=010	$VREG1OUT - VD * (VRON0 + 13R) / sumRN$	VN3
	KN0[2:0]=011	$VREG1OUT - VD * (VRON0 + 17R) / sumRN$	VN4
	KN0[2:0]=100	$VREG1OUT - VD * (VRON0 + 21R) / sumRN$	VN5
	KN0[2:0]=101	$VREG1OUT - VD * (VRON0 + 25R) / sumRN$	VN6
	KN0[2:0]=110	$VREG1OUT - VD * (VRON0 + 29R) / sumRN$	VN7
	KN0[2:0]=111	$VREG1OUT - VD * (VRON0 + 33R) / sumRN$	VN8
VgN8	KN1[2:0]=000	$VREG1OUT - VD * (VRON0 + 33R + VRCN0) / sumRN$	VN9
	KN1[2:0]=001	$VREG1OUT - VD * (VRON0 + 34R + VRCN0) / sumRN$	VN10
	KN1[2:0]=010	$VREG1OUT - VD * (VRON0 + 35R + VRCN0) / sumRN$	VN11
	KN1[2:0]=011	$VREG1OUT - VD * (VRON0 + 36R + VRCN0) / sumRN$	VN12
	KN1[2:0]=100	$VREG1OUT - VD * (VRON0 + 37R + VRCN0) / sumRN$	VN13
	KN1[2:0]=101	$VREG1OUT - VD * (VRON0 + 38R + VRCN0) / sumRN$	VN14
	KN1[2:0]=110	$VREG1OUT - VD * (VRON0 + 39R + VRCN0) / sumRN$	VN15
	KN1[2:0]=111	$VREG1OUT - VD * (VRON0 + 40R + VRCN0) / sumRN$	VN16
VgN20	KN2[2:0]=000	$VREG1OUT - VD * (VRON0 + 45R + VRCN0) / sumRN$	VN17
	KN2[2:0]=001	$VREG1OUT - VD * (VRON0 + 46R + VRCN0) / sumRN$	VN18
	KN2[2:0]=010	$VREG1OUT - VD * (VRON0 + 47R + VRCN0) / sumRN$	VN19
	KN2[2:0]=011	$VREG1OUT - VD * (VRON0 + 48R + VRCN0) / sumRN$	VN20
	KN2[2:0]=100	$VREG1OUT - VD * (VRON0 + 49R + VRCN0) / sumRN$	VN21
	KN2[2:0]=101	$VREG1OUT - VD * (VRON0 + 50R + VRCN0) / sumRN$	VN22
	KN2[2:0]=110	$VREG1OUT - VD * (VRON0 + 51R + VRCN0) / sumRN$	VN23
	KN2[2:0]=111	$VREG1OUT - VD * (VRON0 + 52R + VRCN0) / sumRN$	VN24
VgN43	KN3[2:0]=000	$VREG1OUT - VD * (VRON0 + 68R + VRCN0) / sumRN$	VN25
	KN3[2:0]=001	$VREG1OUT - VD * (VRON0 + 69R + VRCN0) / sumRN$	VN26
	KN3[2:0]=010	$VREG1OUT - VD * (VRON0 + 70R + VRCN0) / sumRN$	VN27
	KN3[2:0]=011	$VREG1OUT - VD * (VRON0 + 71R + VRCN0) / sumRN$	VN28
	KN3[2:0]=100	$VREG1OUT - VD * (VRON0 + 72R + VRCN0) / sumRN$	VN29
	KN3[2:0]=101	$VREG1OUT - VD * (VRON0 + 73R + VRCN0) / sumRN$	VN30
	KN3[2:0]=110	$VREG1OUT - VD * (VRON0 + 74R + VRCN0) / sumRN$	VN31
	KN3[2:0]=111	$VREG1OUT - VD * (VRON0 + 75R + VRCN0) / sumRN$	VN32
VgN55	KN4[2:0]=000	$VREG1OUT - VD * (VRON0 + 80R + VRCN0) / sumRN$	VN33
	KN4[2:0]=001	$VREG1OUT - VD * (VRON0 + 81R + VRCN0) / sumRN$	VN34
	KN4[2:0]=010	$VREG1OUT - VD * (VRON0 + 82R + VRCN0) / sumRN$	VN35
	KN4[2:0]=011	$VREG1OUT - VD * (VRON0 + 83R + VRCN0) / sumRN$	VN36
	KN4[2:0]=100	$VREG1OUT - VD * (VRON0 + 84R + VRCN0) / sumRN$	VN37
	KN4[2:0]=101	$VREG1OUT - VD * (VRON0 + 85R + VRCN0) / sumRN$	VN38
	KN4[2:0]=110	$VREG1OUT - VD * (VRON0 + 86R + VRCN0) / sumRN$	VN39
	KN4[2:0]=111	$VREG1OUT - VD * (VRON0 + 87R + VRCN0) / sumRN$	VN40
VgN62	KN5[2:0]=000	$VREG1OUT - VD * (VRON0 + 87R + VRCN0 + VRCN1) / sumRN$	VN41
	KN5[2:0]=001	$VREG1OUT - VD * (VRON0 + 91R + VRCN0 + VRCN1) / sumRN$	VN42
	KN5[2:0]=010	$VREG1OUT - VD * (VRON0 + 95R + VRCN0 + VRCN1) / sumRN$	VN43
	KN5[2:0]=011	$VREG1OUT - VD * (VRON0 + 99R + VRCN0 + VRCN1) / sumRN$	VN44
	KN5[2:0]=100	$VREG1OUT - VD * (VRON0 + 103R + VRCN0 + VRCN1) / sumRN$	VN45
	KN5[2:0]=101	$VREG1OUT - VD * (VRON0 + 107R + VRCN0 + VRCN1) / sumRN$	VN46
	KN5[2:0]=110	$VREG1OUT - VD * (VRON0 + 111R + VRCN0 + VRCN1) / sumRN$	VN47
	KN5[2:0]=111	$VREG1OUT - VD * (VRON0 + 115R + VRCN0 + VRCN1) / sumRN$	VN48
VgN63	—	$VREG1OUT - VD * (VRON0 + 120R + VRCN0 + VRCN1) / sumRN$	VN49

Sum of positive resistor sumRP = 128R + VROP0 + VROP1 + VRCP0 + VRCP1

Sum of negative resistor sumRN = 128R + VRON0 + VRON1 + VRCN0 + VRCN1

Voltage difference VD = (VREG1OUT – VGS)

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VgN0	V32	V43+(V20-V43)*(11/23)
V1	VgN1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VgN8	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VgN43
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VgN20	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VgN55
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VgN62
V31	V43+(V20-V43)*(12/23)	V63	VgN63

Relationship between RAM data and voltage output levels (REV = "0")

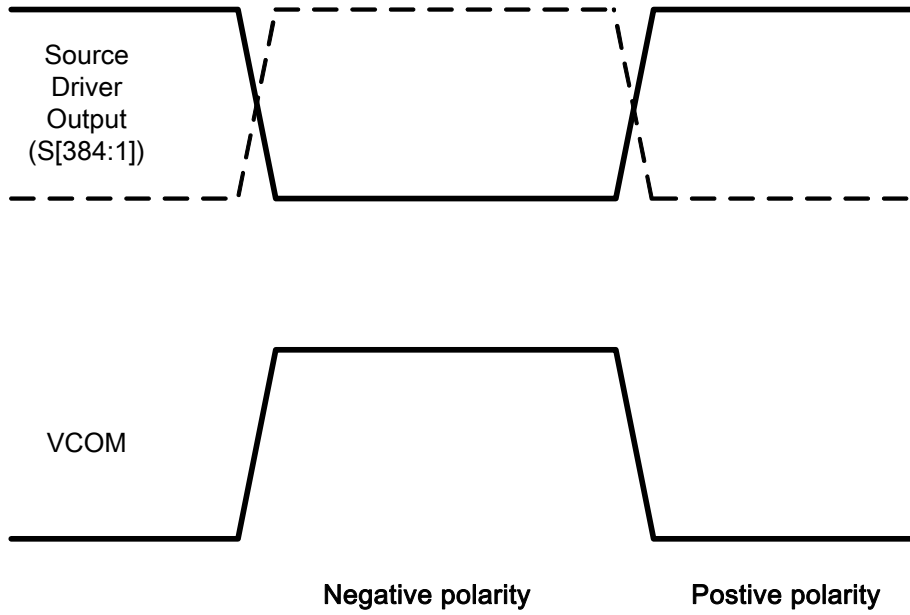


Figure 39 Relationship between Source Output and VCOM

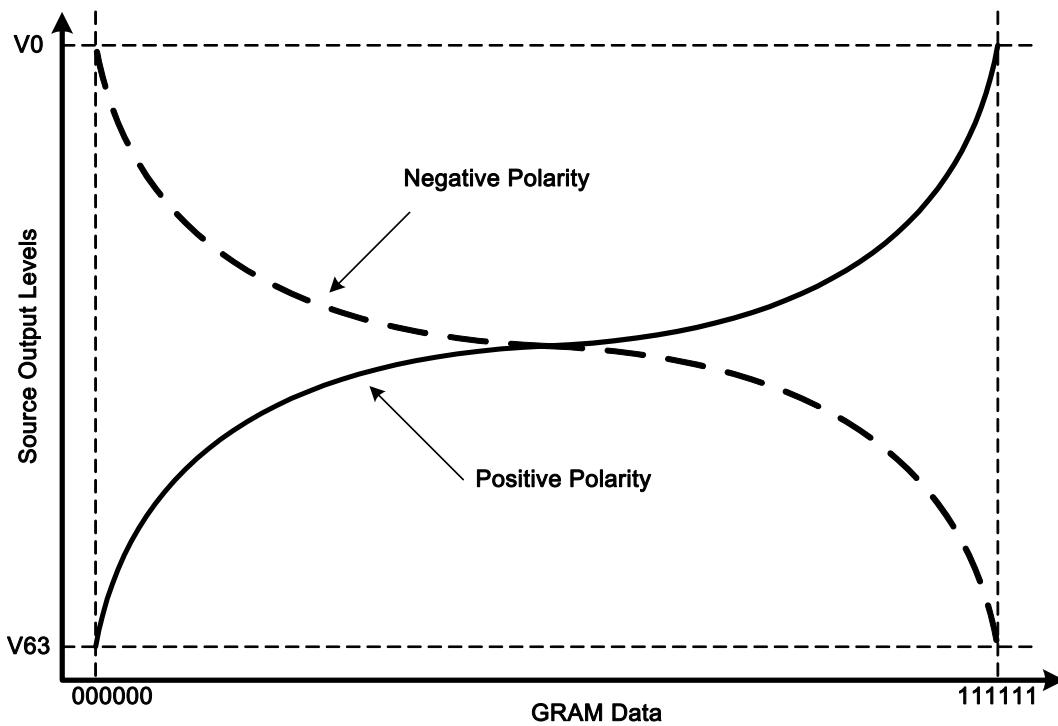
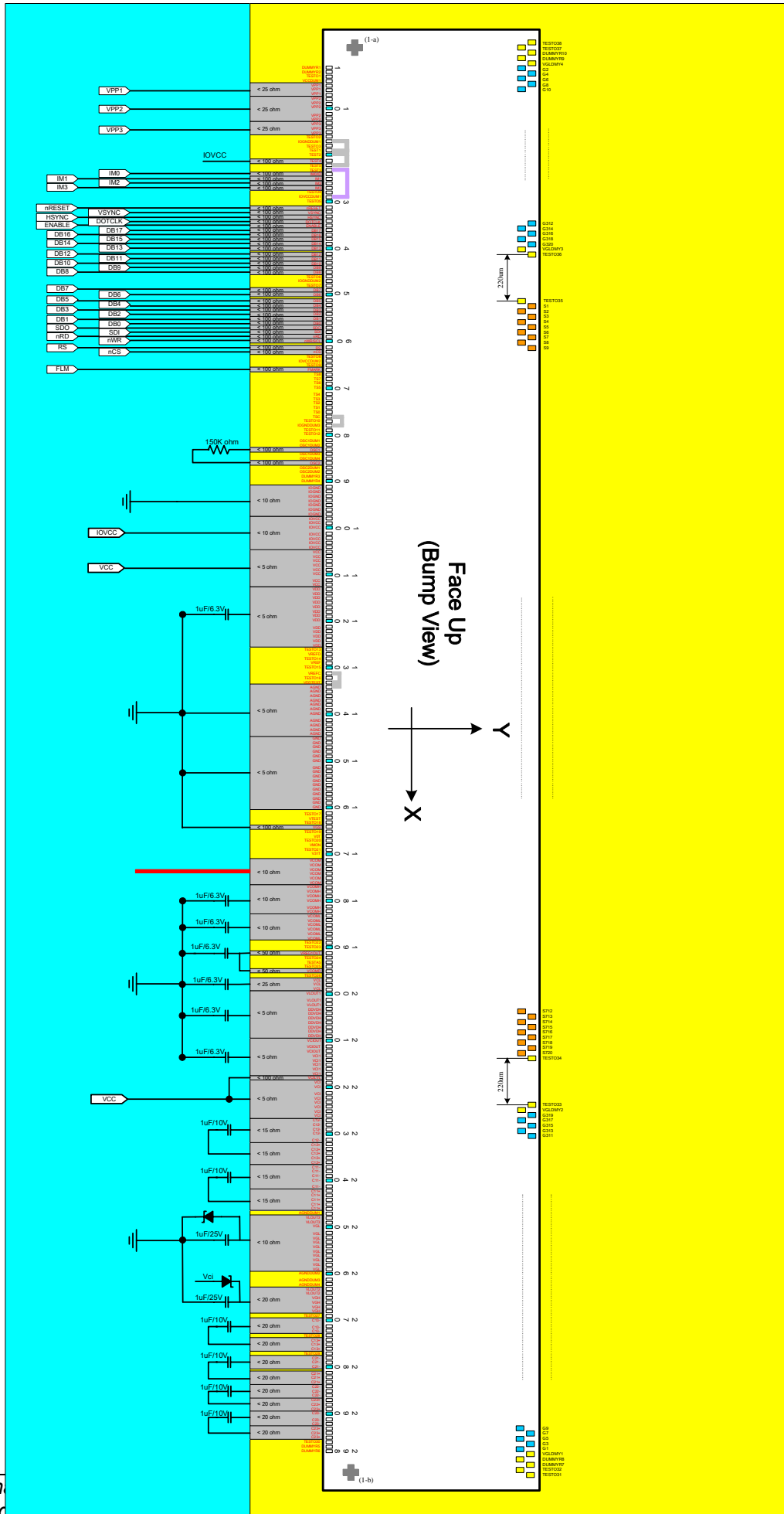


Figure 40 Relationship between GRAM Data and Output Level



## 12. Application

### 12.1. Configuration of Power Supply Circuit



**Figure 41 Power Supply Circuit Block**

The following table shows specifications of external elements connected to the ILI9320's power supply circuit.

Items	Recommended Specification	Pin connection
<b>Capacity</b> 1 $\mu$ F (B characteristics)	6V	VREG1OUT, VCI1, VDD, VCL, VCOMH, VCOML, C11+/-, C12+/-
	10V	DDVDH, C21+/-, C22+/-
	25V	VGH, VGL
<b>Schottky diode</b>	$V_F < 0.4V/20mA$ at 25°C, $V_R \geq 30V$ (Recommended diode: HSC226)	(AGND – VGL), (Vci – VGH), (Vci – DDVDH)
<b>Variable resistor</b>	> 200 k $\Omega$	VCOMR

## 12.2. Display ON/OFF Sequence

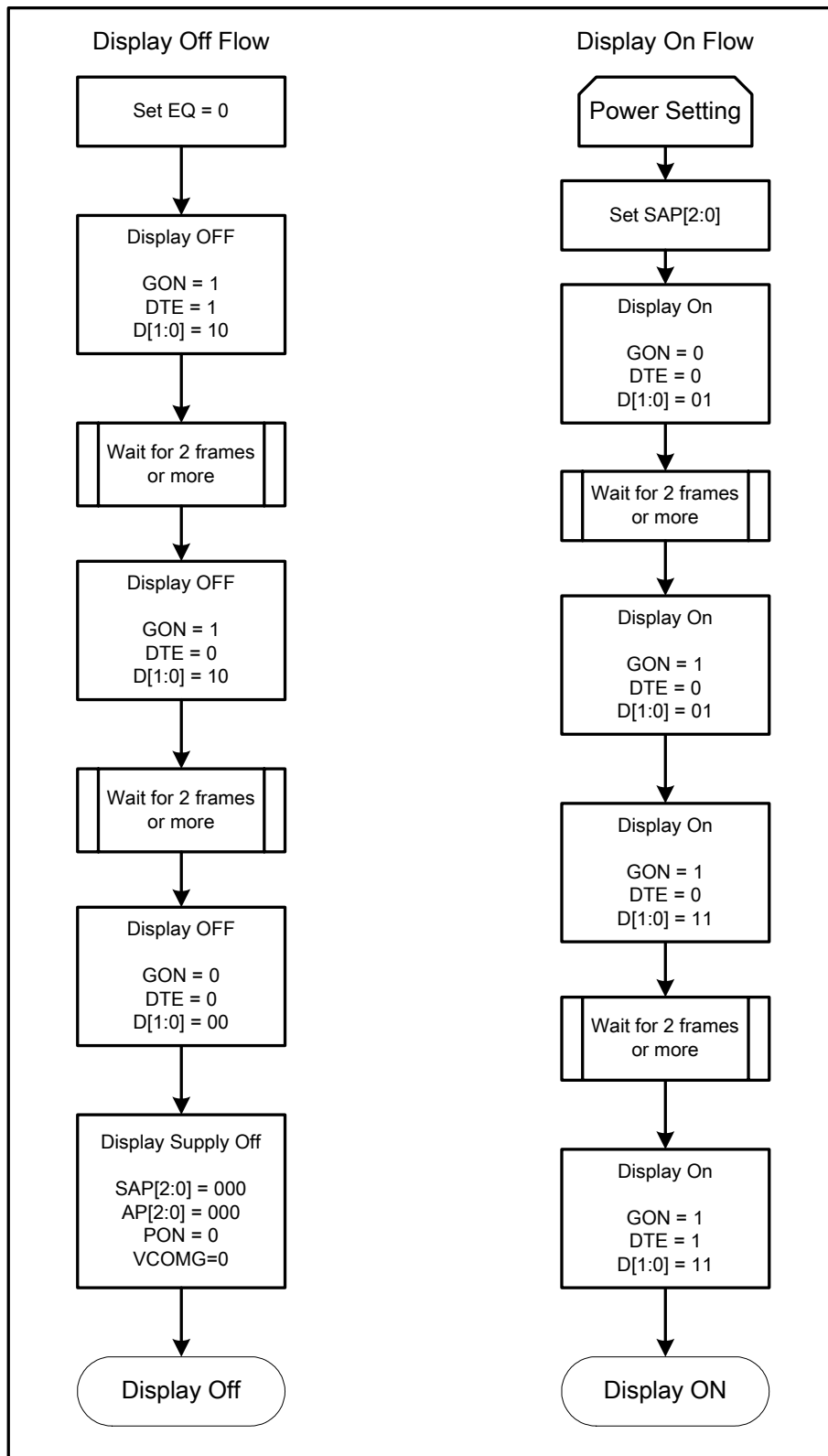
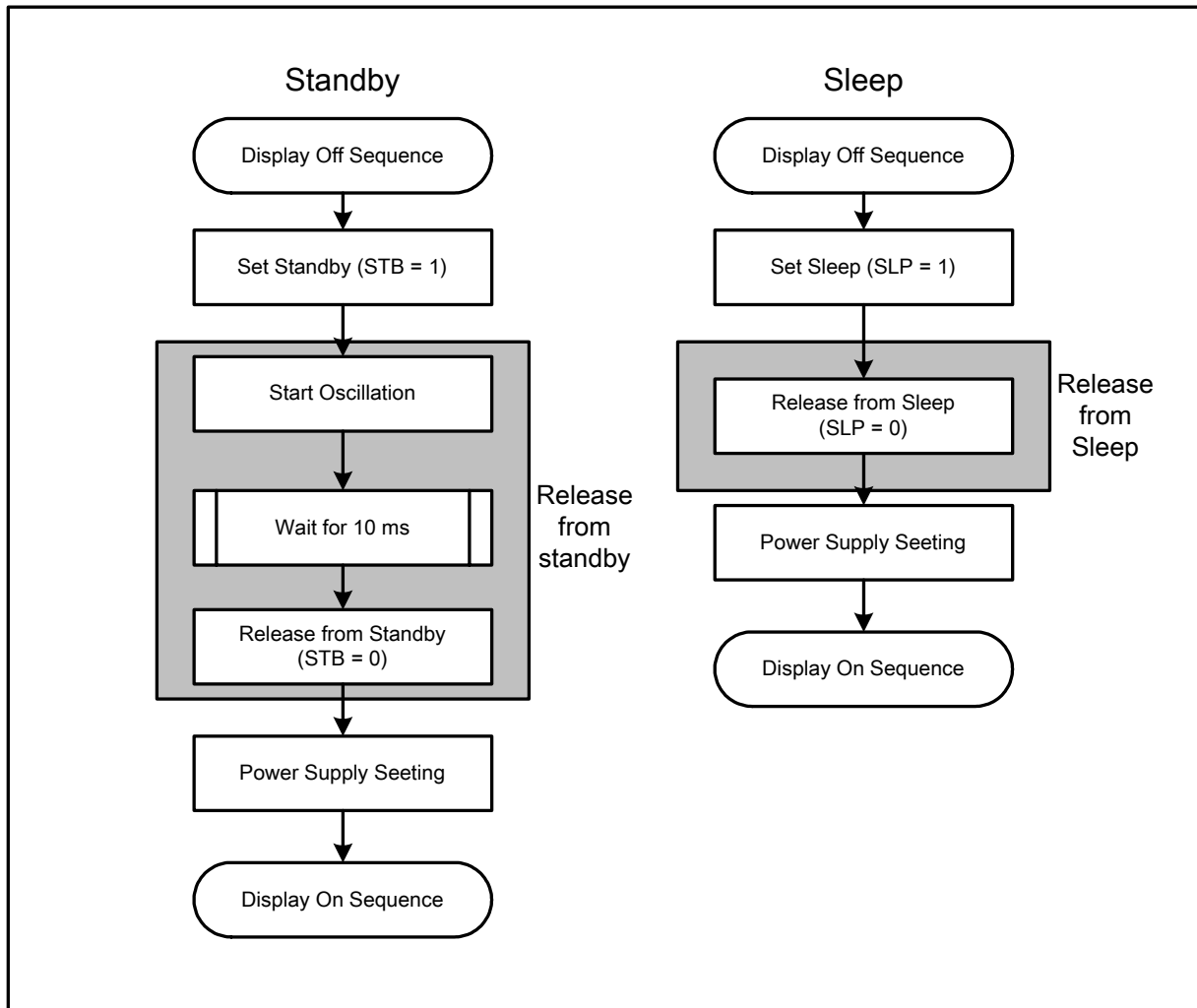


Figure 42 Display On/Off Register Setting Sequence

### 12.3. Standby and Sleep Mode



**Figure 43 Standby/Sleep Mode Register Setting Sequence**

## 12.4. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.

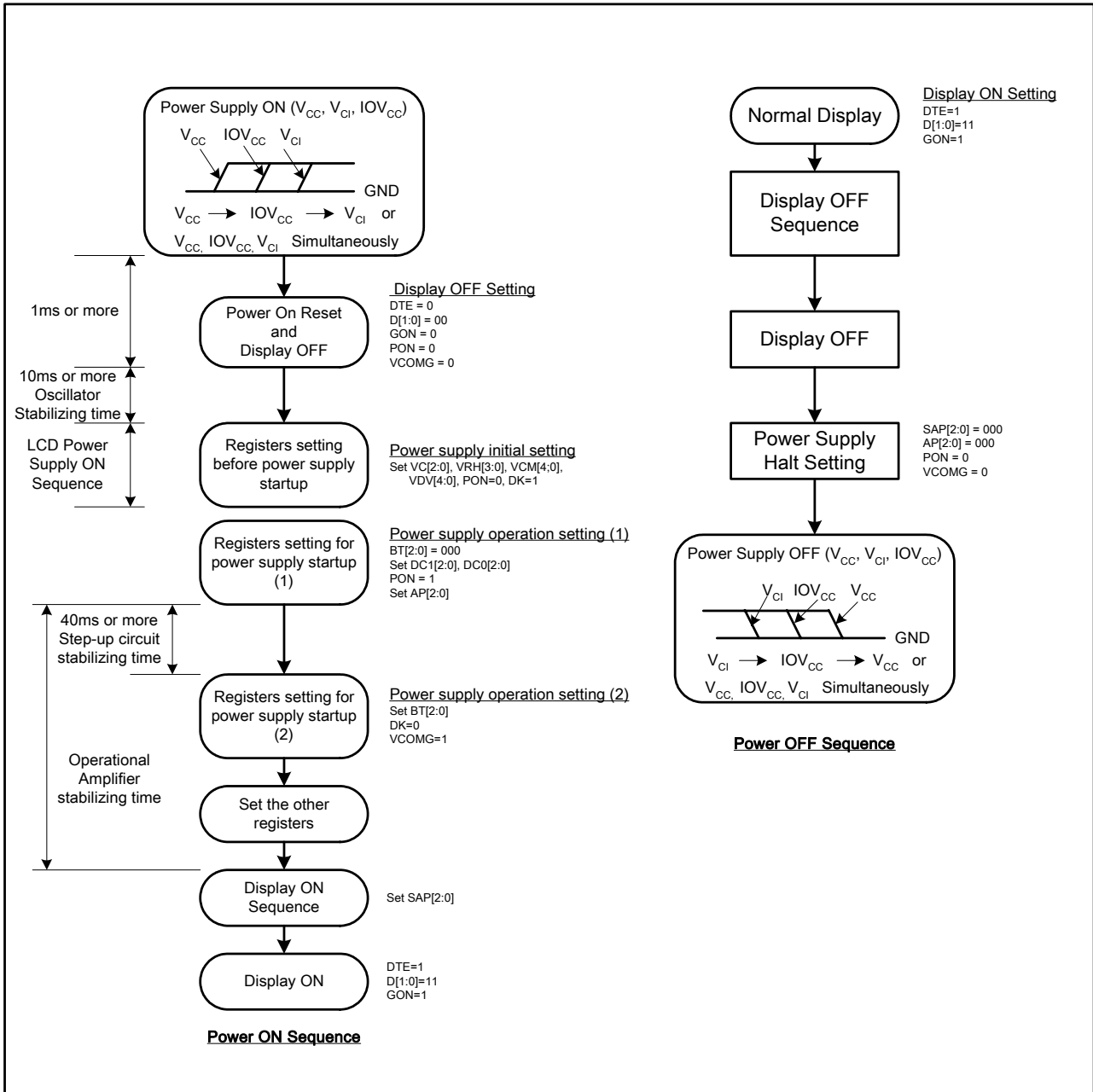
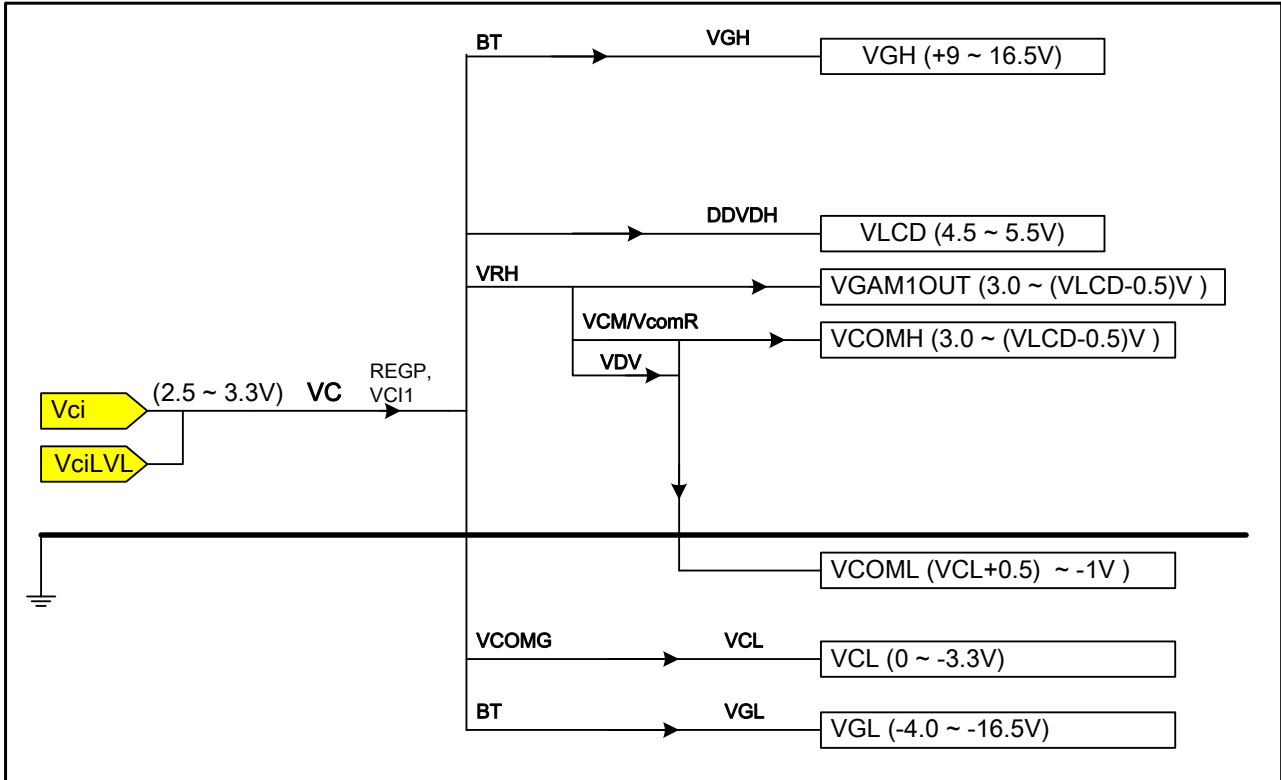


Figure 44 Power Supply ON/OFF Sequence

## 12.5. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ILI9320 are as follows.



**Figure 45 Voltage Configuration Diagram**

Note: The DDVDH, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective outputs. The voltage levels in the following relationships  $(DDVDH - VREG1OUT) > 0.5V$ ,  $(VCOML1 - VCL) > 0.5V$ ,  $(VCOML2 - VCL) > 0.5V$  are the actual voltage levels. When the alternating cycles of VCOM are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.

## 12.6. Applied Voltage to the TFT panel

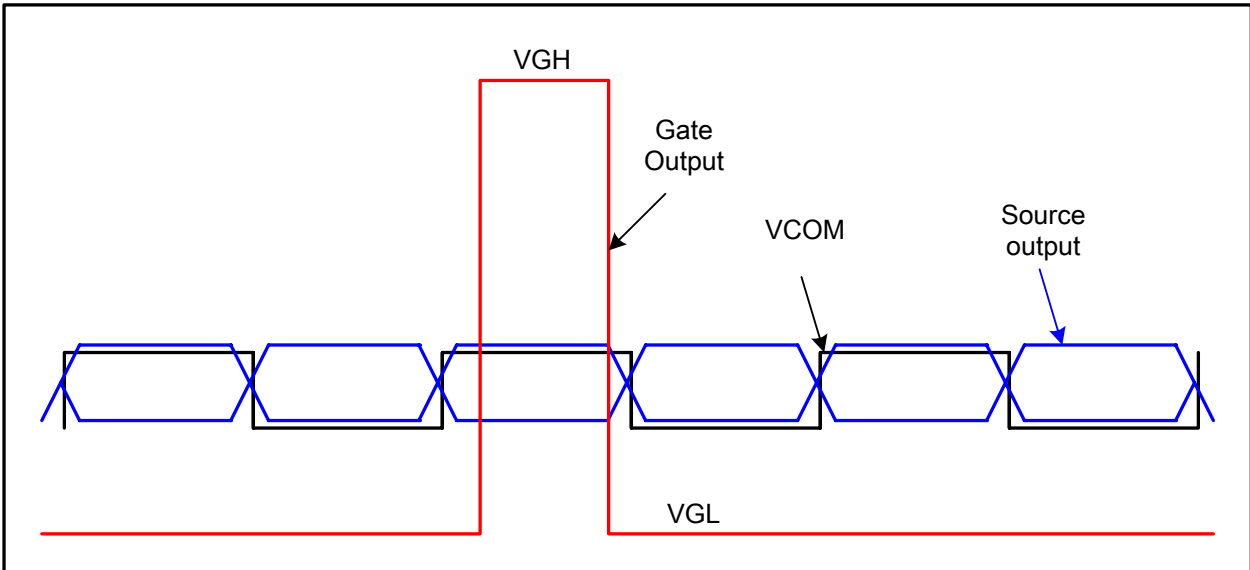


Figure 46 Voltage Output to TFT LCD Panel

## 12.7. Oscillator

ILI9320 generates oscillation with the ILI9320's internal RC oscillators by placing an external resistor between the OSC1 and OSC2 pins. The oscillation frequency varies with resistance value of external resistor, wiring distance, and operating supply voltage. For example, placing a  $R_{osc}$  resistor of larger resistance value or lower the supply voltage level will generate a lower oscillation frequency. See the "Notes to Electrical Characteristics" section for the relationship between resistance value of  $R_{osc}$  resistor and oscillation frequency.

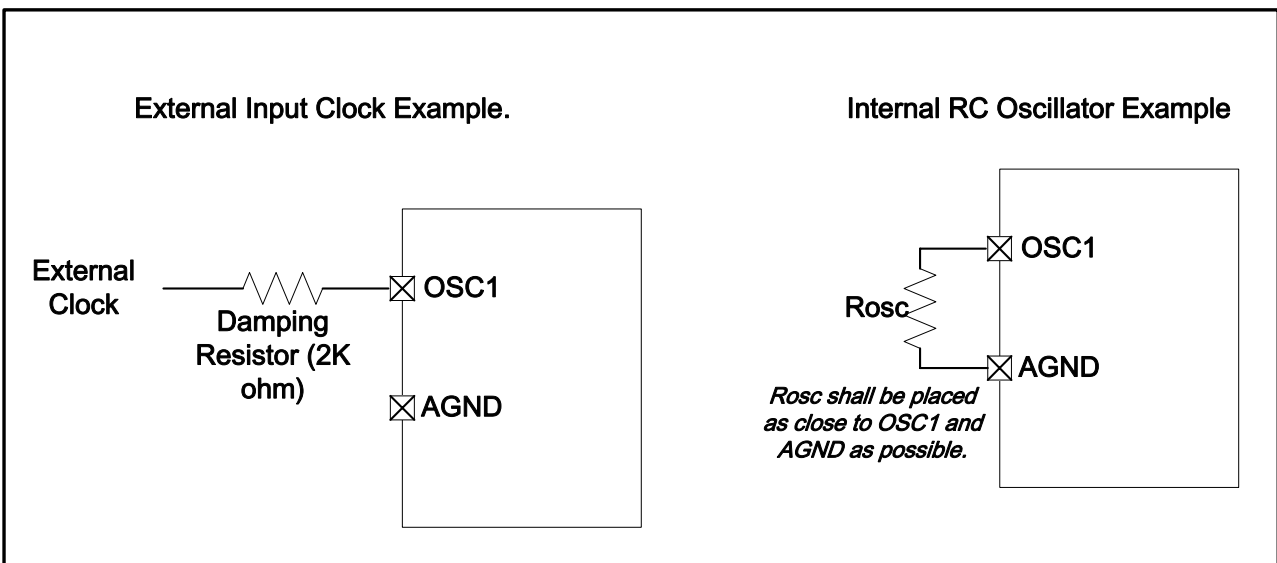


Figure 47 Oscillation Connection



## 12.8. Frame Rate Adjustment

The ILI9320 has a frame frequency adjustment function. The frame frequency for driving LCDs can be adjusted by registers (using the DIV, RTN bits) without changing the oscillation frequency.

To switch frame frequencies between when displaying a moving picture and when displaying a still picture, set a high oscillation frequency in advance. By doing so, it becomes possible to set a low frame frequency when displaying a still picture for saving power consumption and to set a high frame frequency when displaying a moving picture.

### Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following formula. The frame frequency is adjusted by register using the 1H period adjustment bits (RTN bits) and the operation clock division bits (DIV bits).

Formula to calculate frame frequency

$$\text{Formula rate} = \frac{f_{osc.}}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Lines} + \text{BP} + \text{FP})}$$

$f_{osc.}$  : frequency of RC oscillation.  
 Clock cycles per line : RTN bits  
 Division ratio : DIV bits  
 Lines : number of lines for driving the LCD panel.  
 FP: Front porch lines  
 BP; Back porch lines

### Example of Calculation: when maximum frame frequency = 60 Hz

Number of lines to drive the LCD: 320 lines

1H period: 16 clock cycle (RTNI[4:0] = "00000")

Operational clock division ratio: 1/1

$$f_{osc} = 60 \text{ Hz} \times (0 + 16) \text{ clock} \times 1/1 \times (320 + 16) \text{ lines} = 322.56 \text{ (kHz)}$$

In this case, the RC oscillation frequency is 322.56kHz. Adjust the external resistor of the RC oscillator to 322.56kHz.

## 12.9. Partial Display Function

The ILI9320 allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers.

The following example shows the setting for partial display function:

Base Image Display Setting	
BASEE	0
NL[5:0]	6'h27

Partial Image 1 Display Setting	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080
Partial Image 2 Display Setting	
PTDE1	1
PTSA1[8:0]	9'h020
PTEA1[8:0]	9'h02F
PTDP1[8:0]	9'h0C0

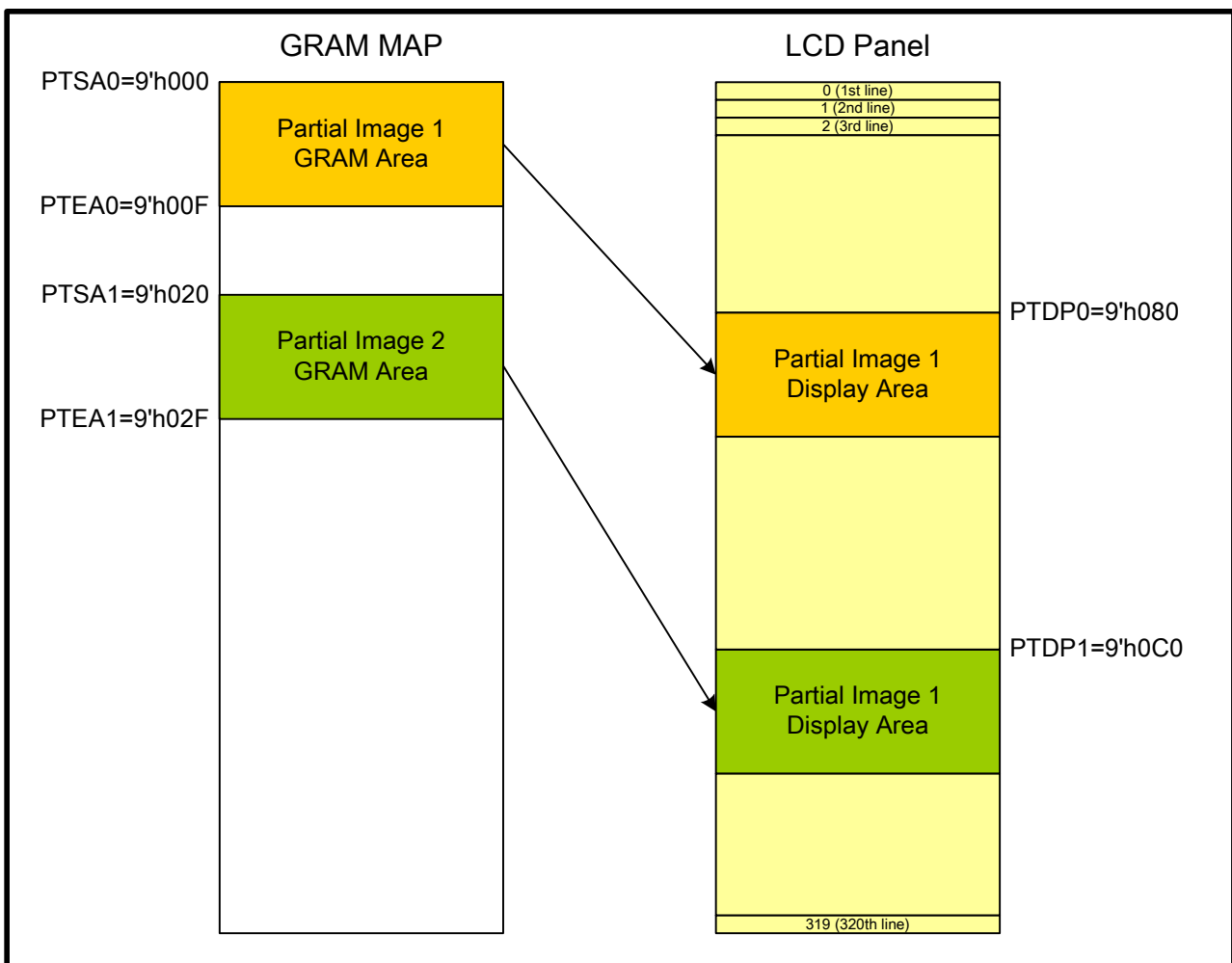


Figure 48 Partial Display Example

## 12.10. Resizing Function

ILI9320 supports resizing function (x1/2, x1/4), which is performed when writing image data to GRAM. The

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resizing function is enabled by setting a window address area and the RSZ bit which represents the resizing factor (x1/2, x1/4) of image. The resizing function allows the system to transfer the original-size image data into the GRAM with resized image data.

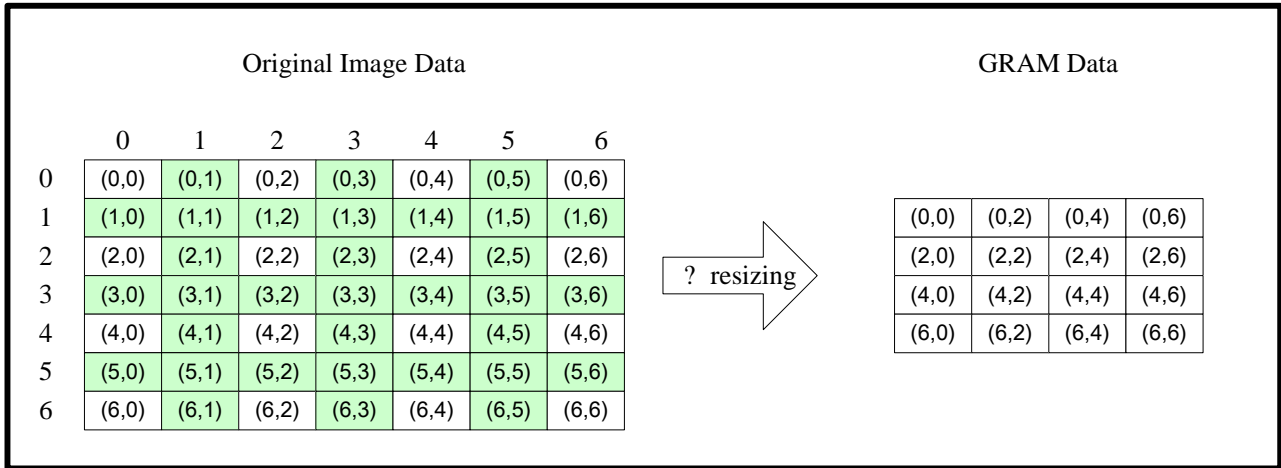


Figure 49 Data transfer in resizing

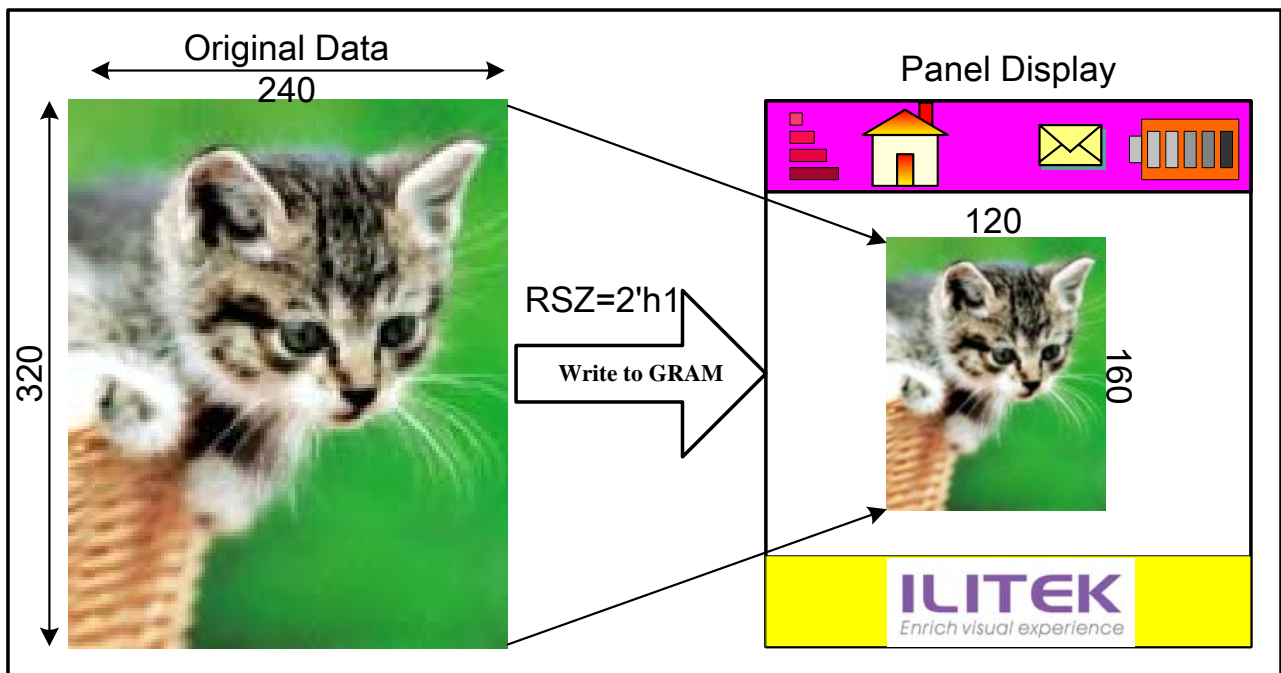
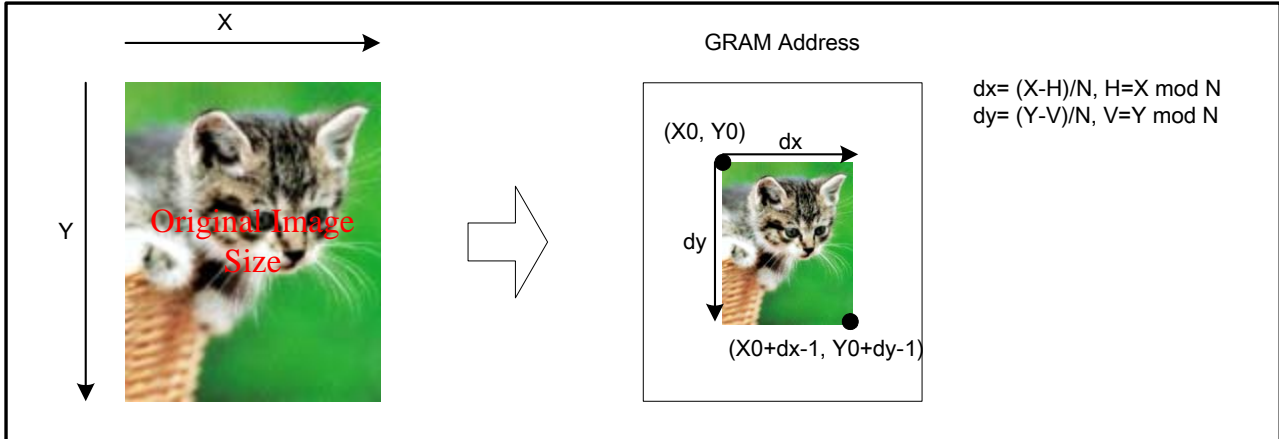


Figure 50 Resizing Example

Original Image Size (X × Y)	Resized Image Resolution	
	1/2 (RSZ=2'h1)	1/4 (RSZ=2'h3)
640 × 480	320 × 240	160 × 120
352 × 288	176 × 144	88 × 72
320 × 240	160 × 120	80 × 60
176 × 144	88 × 72	44 × 36
120 × 160	60 × 80	30 × 40
132 × 132	66 × 66	33 × 33

The RSZ bit sets the resizing factor of an image. When setting a window address area in the internal GRAM, the GRAM window address area must fit the size of resized image. The following example show the resizing setting.



Original image data number in horizontal direction		X
Original image data number in Vertical direction		Y
Resizing Ration		1/N
Resizing Setting	RSZ	N-1
Remainder pixels in horizontal direction	RCH	H
Remainder pixels in vertical direction	RCV	V
GRAM writing start address	AD	(x0, y0)
GRAM window setting	HSA	x0
	HEA	x0+dx-1
	VSA	y0
	VEA	y0+dy-1

## 13. Electrical Characteristics

### 13.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9320 is used out of the absolute maximum ratings, the ILI9320 may be permanently damaged. To use the ILI9320 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9320 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	VCC, IOVCC	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (1)	VCI - AGND	V	-0.3 ~ + 4.6	1, 4
Power supply voltage (1)	DDVDH - AGND	V	-0.3 ~ + 6.0	1, 4
Power supply voltage (1)	AGND -VCL	V	-0.3 ~ + 4.6	1
Power supply voltage (1)	DDVDH - VCL	V	-0.3 ~ + 9.0	1, 5
Power supply voltage (1)	VGH - AGND	V	-0.3 ~ + 18.5	1, 5
Power supply voltage (1)	AGND - VGL	V	-0.3 ~ + 18.5	1, 6
Input voltage	Vt	V	-0.3 ~ VCC+ 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	8, 9
Storage temperature	Tstg	°C	-55 ~ + 110	8, 9

Notes:

1. VCC, DGND must be maintained
2. (High) (VCC = VCC) ≥ DGND (Low), (High) IOVCC ≥ DGND (Low).
3. Make sure (High) VCI ≥ DGND (Low).
4. Make sure (High) DDVDH ≥ ASSD (Low).
5. Make sure (High) DDVDH ≥ VCL (Low).
6. Make sure (High) VGH ≥ ASSD (Low).
7. Make sure (High) ASSD ≥ VGL (Low).
8. For die and wafer products, specified up to 85°C.
9. This temperature specifications apply to the TCP package

### 13.2. DC Characteristics

(VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V, Ta= -40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V <sub>IH</sub>	V	VCC= 1.8 ~ 3.3V	0.8*IOVCC	-	IOVCC	-
Input low voltage	V <sub>IL</sub>	V	VCC= 1.8 ~ 3.3V	-0.3	-	0.2*IOVCC	-
Output high voltage(1) ( DB0-17 Pins)	V <sub>OH1</sub>	V	IOH = -0.1 mA	0.8*IOVCC	-	-	-
Output low voltage ( DB0-17 Pins)	V <sub>OL1</sub>	V	IOVCC=1.65~3.3V VCC= 2.4 ~ 3.3V IOL = 0.1mA	-	-	0.2*IOVCC	-
I/O leakage current	I <sub>LI</sub>	μA	Vin = 0 ~ VCC	-0.1	-	0.1	-
Current consumption during normal operation (V <sub>CC</sub> - DGND)	I <sub>OP</sub>	μA	VCC=2.8V, Ta=25°C, fOSC = 376KHz ( Line) GRAM data = 0000h	-	100 (VCC)	-	-
Current consumption during standby mode (V <sub>CC</sub> - DGND)	I <sub>ST</sub>	μA	VCC=2.8V, Ta=25 °C	-	5	10	-
LCD Drive Power Supply Current ( DDVDH-DGND )	ILCD	mA	VCC=2.8V, VREG1OUT =4.8V DDVDH=5.0V, fOSC = 376KHz (320 line), Ta=25 °C, GRAM data = 0000h, REV="0", SAP="001", ON4-0="0", OP4-0="0", MP52-00="0", MN52-00="0", CP12-00="0" CN12-00="0"	-	3.0	-	-
LCD Driving Voltage ( DDVDH-DGND )	DDVDH	V	-	4.5	-	6	-
Output voltage deviation		mV	-	-	5	-	-
Dispersion of the Average Output Voltage	V	mV	-	-10	-	10	-

### 13.3. Clock Characteristics

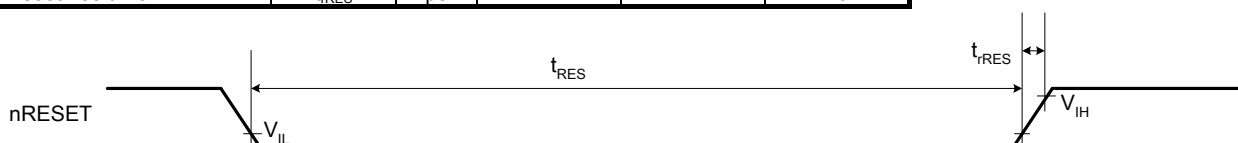
VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
External Clock Frequency	f <sub>cp</sub>	VCC = 2.4 ~ 3.3V	275	335	395	KHz
External Clock Duty	f <sub>Duty</sub>	VCC = 2.4 ~ 3.3V	45	50	55	
External Clock Rising Time	Trcp	VCC = 2.4 ~ 3.3V	-	-	0.2	μs
External Clock Falling Time	Tfcp	VCC = 2.4 ~ 3.3V	-	-	0.2	μs
RC oscillation clock	f <sub>OSC</sub>	Rf = 130KΩ, VCC = 2.8V	275	335	395	KHz

### 13.4. Reset Timing Characteristics

Reset Timing Characteristics (VCC = 1.8 ~ 3.3 V, IOVCC = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t <sub>RES</sub>	ms	1	-	-
Reset rise time	t <sub>RES</sub>	μs	-	-	10



### 13.5. LCD Driver Output Characteristics

Item	Symbol	Timing diagram	Min.	Typ.	Max.	Unit
Driver output delay time	tdd	VCC=2.8V, DDVDH=5.0V, VREG1OUT =4.8V, RC oscillation: fosc =376kHz (320 lines), Ta=25°C REV=0, SAP=010, AP=010, 0N14-00=0, 0P14-00=0, MP52-00=0, MN52-00=0, CP12-00=0, CN12-00=0, Load resistance R=10kΩ, Load capacitance C=20pF • when the level changes from a same grayscale level on all pins • Time to reach +/-35mV when VCOM polarity inverts	-	35	-	μs

## 13.6. AC Characteristics

### 13.6.1. i80-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t <sub>CYCW</sub>	ns	100	-	-
	Read	t <sub>CYCR</sub>	ns	300	-	-
Write low-level pulse width	PW <sub>LW</sub>	ns	50	-	500	-
Write high-level pulse width	PW <sub>HW</sub>	ns	50	-	-	-
Read low-level pulse width	PW <sub>LR</sub>	ns	150	-	-	-
Read high-level pulse width	PW <sub>HR</sub>	ns	150	-	-	-
Write / Read rise / fall time	t <sub>WRr</sub> /t <sub>WRf</sub>	ns	-	-	25	-
Setup time	Write ( RS to nCS, E/nWR )	t <sub>AS</sub>	ns	10	-	-
	Read ( RS to nCS, RW/nRD )			5	-	-
Address hold time	t <sub>AH</sub>	ns	5	-	-	-
Write data set up time	t <sub>DSW</sub>	ns	10	-	-	-
Write data hold time	t <sub>H</sub>	ns	15	-	-	-
Read data delay time	t <sub>DDR</sub>	ns	-	-	100	-
Read data hold time	t <sub>DHR</sub>	ns	5	-	-	-

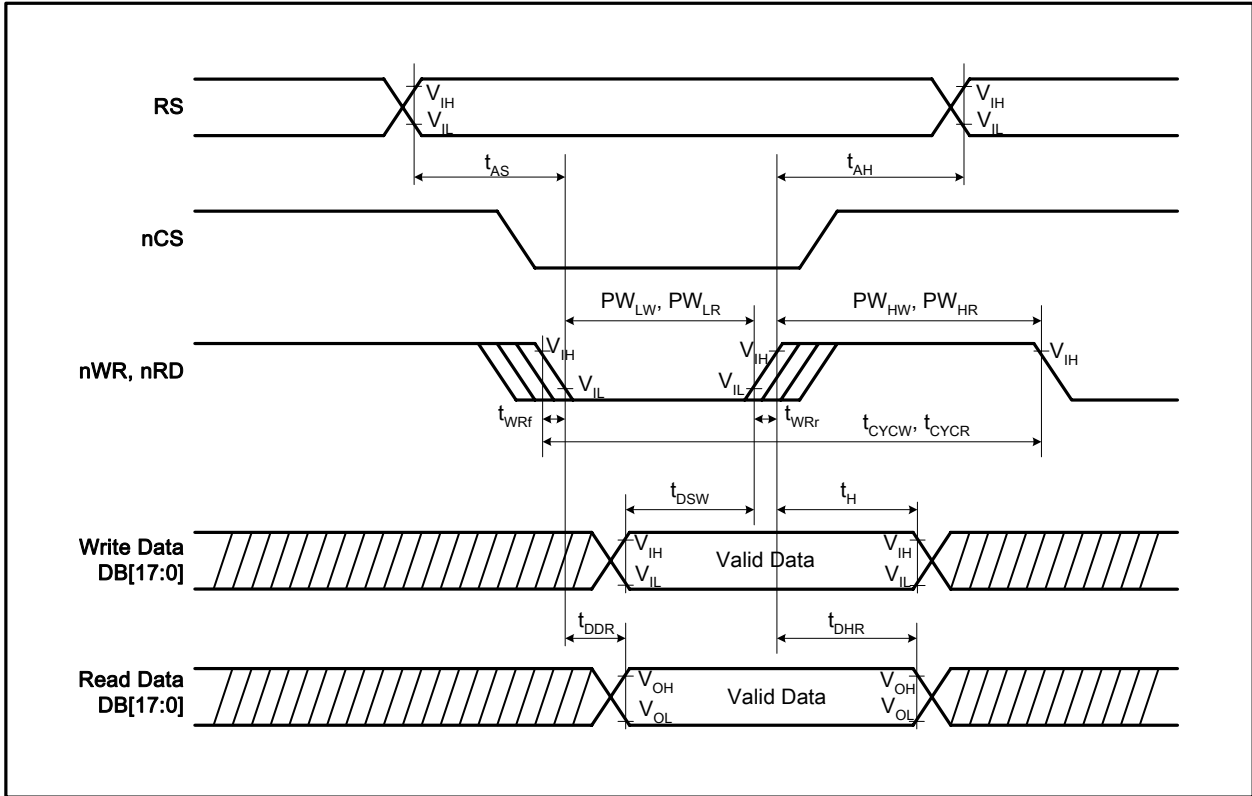


Figure 51 i80-System Bus Timing

### 13.6.2. Serial Data Transfer Interface Timing Characteristics

(IOVCC= 1.653.3V and VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write ( received )	$t_{SCYC}$	$\mu s$	100	-	-
	Read ( transmitted )	$t_{SCYC}$	$\mu s$	200	-	-
Serial clock high – level pulse width	Write ( received )	$t_{SCH}$	ns	40	-	-
	Read ( transmitted )	$t_{SCH}$	ns	100	-	-
Serial clock low – level pulse width	Write ( received )	$t_{SCL}$	ns	40	-	-
	Read ( transmitted )	$t_{SCL}$	ns	100	-	-
Serial clock rise / fall time	$t_{SCr}, t_{SCf}$	ns	-	-	5	
Chip select set up time	$t_{CSU}$	ns	10	-	-	
Chip select hold time	$t_{CH}$	ns	50	-	-	
Serial input data set up time	$t_{SISU}$	ns	20	-	-	
Serial input data hold time	$t_{SIH}$	ns	20	-	-	
Serial output data set up time	$t_{SOD}$	ns	-	-	100	
Serial output data hold time	$t_{SOH}$	ns	5	-	-	



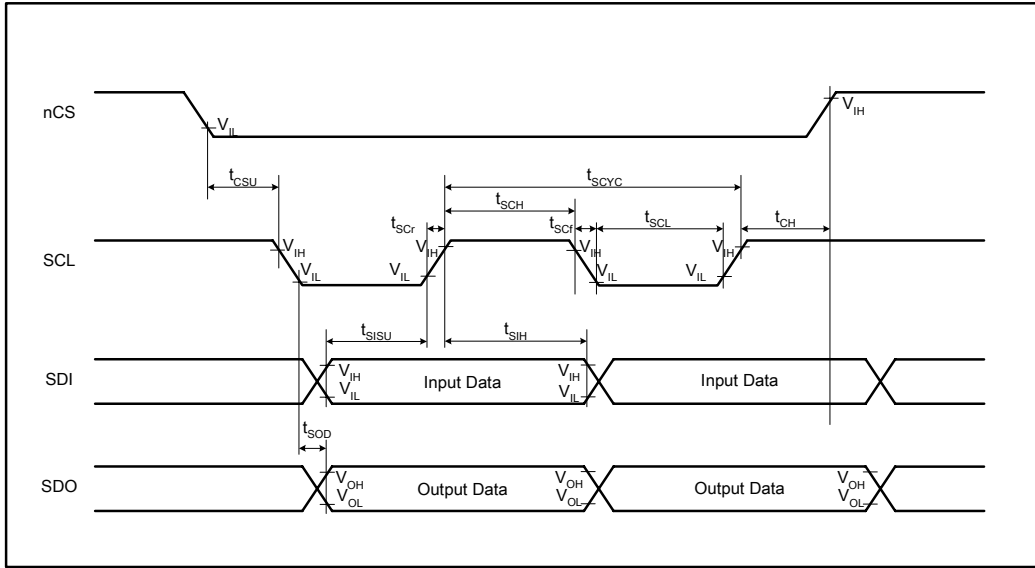


Figure 52 SPI System Bus Timing

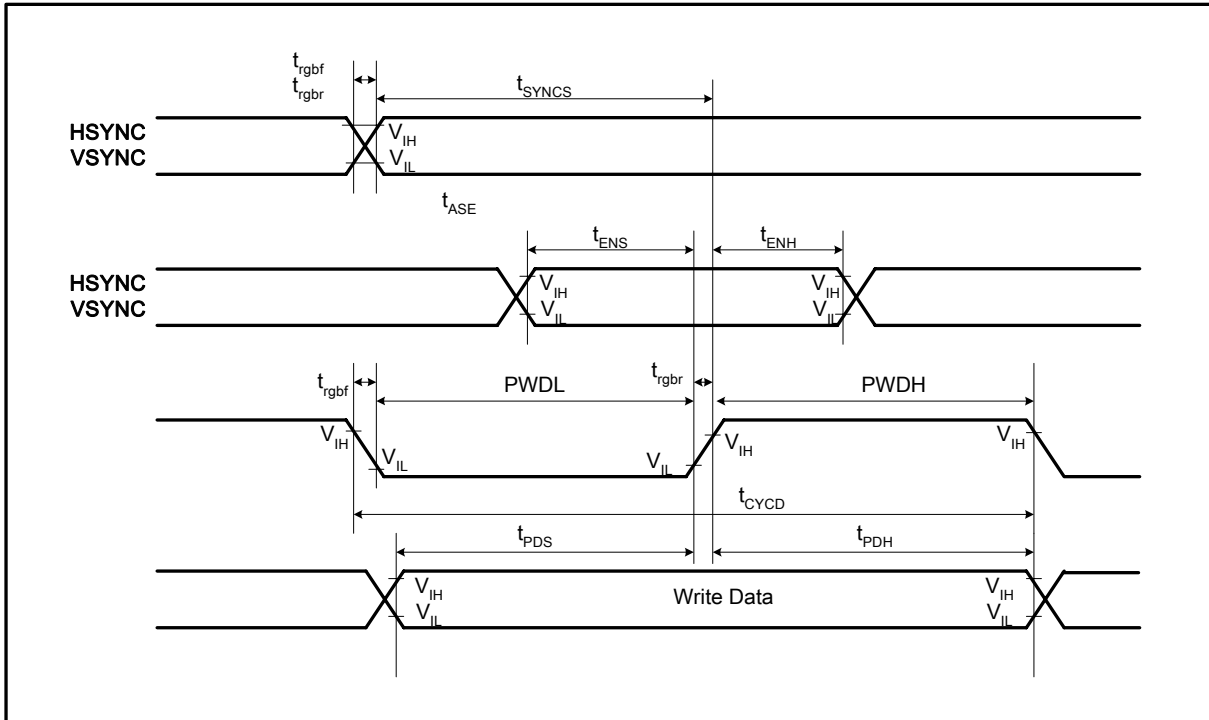
### 13.6.3. RGB Interface Timing Characteristics

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t <sub>SYNCS</sub>	ns	0	-	-	-
ENABLE setup time	t <sub>ENS</sub>	ns	10	-	-	-
ENABLE hold time	t <sub>ENH</sub>	ns	10	-	-	-
PD Data setup time	t <sub>PDs</sub>	ns	10	-	-	-
PD Data hold time	t <sub>PDH</sub>	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t <sub>CYCD</sub>	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t <sub>rghr</sub> , t <sub>rghf</sub>	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t <sub>SYNCS</sub>	ns	0	-	-	-
ENABLE setup time	t <sub>ENS</sub>	ns	10	-	-	-
ENABLE hold time	t <sub>ENH</sub>	ns	10	-	-	-
PD Data setup time	t <sub>PDs</sub>	ns	10	-	-	-
PD Data hold time	t <sub>PDH</sub>	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t <sub>CYCD</sub>	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t <sub>rghr</sub> , t <sub>rghf</sub>	ns	-	-	25	-



**Figure53 RGB Interface Timing**

## 14. Revision History

Version No.	Date	Page	Description
V.01	2006/4/17		New Created