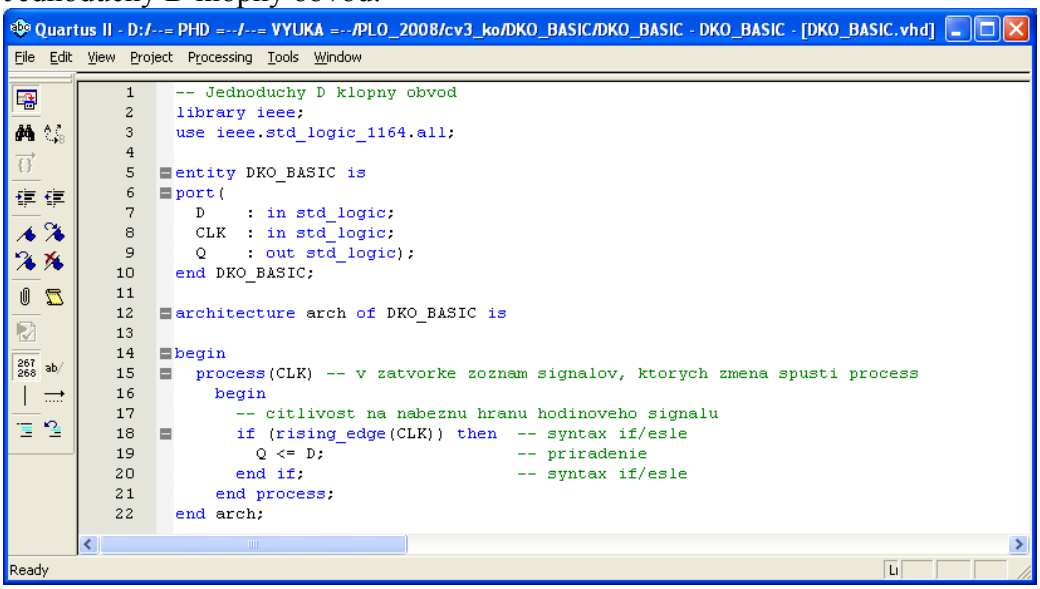
Cvičenie 5
Jednoduché sekvenčné obvody

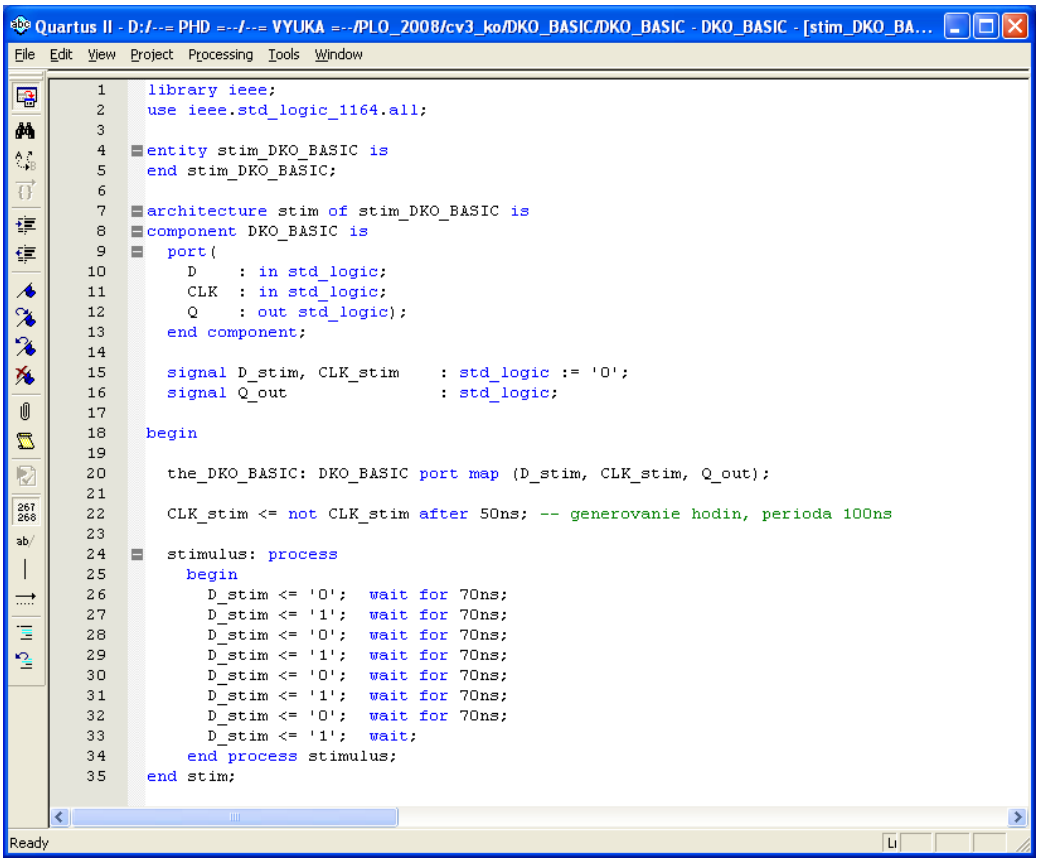
Zadanie:
Odsimulujte (a vyskúšajte na doske) klopné obvody typu D a JK.

Výpisy kódov:
Jednoduchý D klopný obvod:



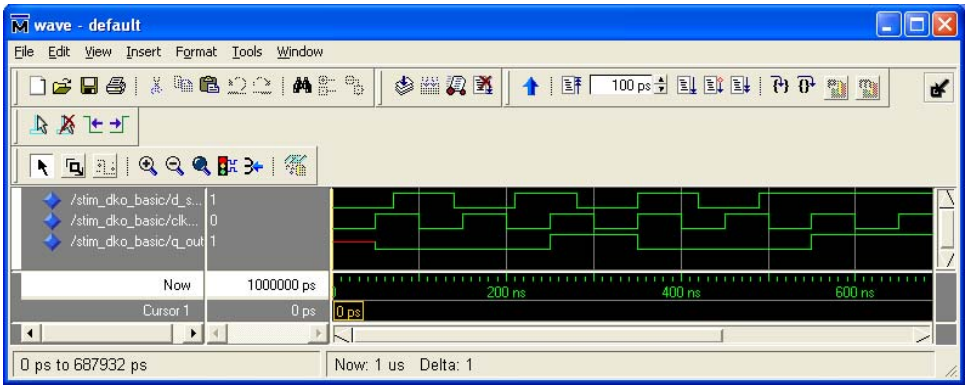

```
1  -- Jednoduchy D klopny obvod
2  library ieee;
3  use ieee.std_logic_1164.all;
4
5  entity DKO_BASIC is
6  port(
7     D     : in std_logic;
8     CLK   : in std_logic;
9     Q     : out std_logic);
10 end DKO_BASIC;
11
12 architecture arch of DKO_BASIC is
13
14 begin
15   process(CLK) -- v zatvorke zoznam signalov, ktorych zmena spusti process
16     begin
17       -- citlivost na nabeznu hranu hodinoveho signalu
18       if (rising_edge(CLK)) then  -- syntax if/esle
19         Q <= D;                   -- priradenie
20       end if;                     -- syntax if/esle
21     end process;
22 end arch;
```

Test bench:

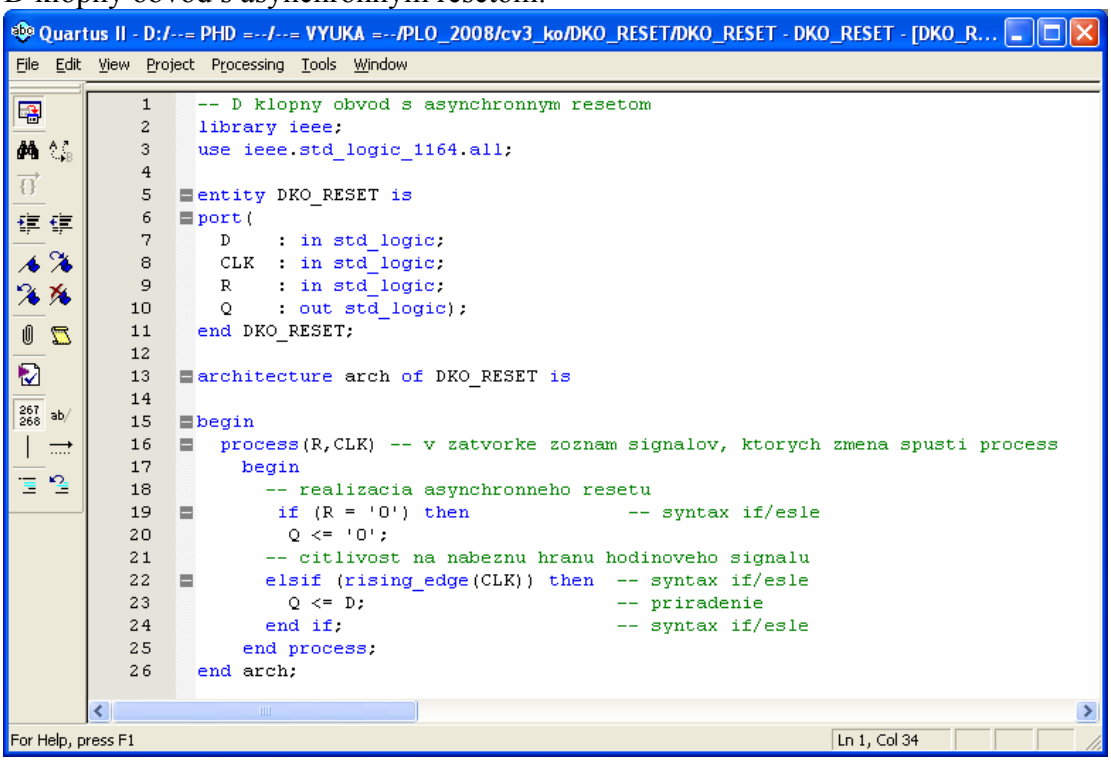



```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity stim_DKO_BASIC is
5  end stim_DKO_BASIC;
6
7  architecture stim of stim_DKO_BASIC is
8  component DKO_BASIC is
9    port(
10     D     : in std_logic;
11     CLK   : in std_logic;
12     Q     : out std_logic);
13   end component;
14
15   signal D_stim, CLK_stim    : std_logic := '0';
16   signal Q_out               : std_logic;
17
18 begin
19
20   the_DKO_BASIC: DKO_BASIC port map (D_stim, CLK_stim, Q_out);
21
22   CLK_stim <= not CLK_stim after 50ns; -- generovanie hodin, perioda 100ns
23
24   stimulus: process
25     begin
26       D_stim <= '0';  wait for 70ns;
27       D_stim <= '1';  wait for 70ns;
28       D_stim <= '0';  wait for 70ns;
29       D_stim <= '1';  wait for 70ns;
30       D_stim <= '0';  wait for 70ns;
31       D_stim <= '1';  wait for 70ns;
32       D_stim <= '0';  wait for 70ns;
33       D_stim <= '1';  wait;
34     end process stimulus;
35 end stim;
```

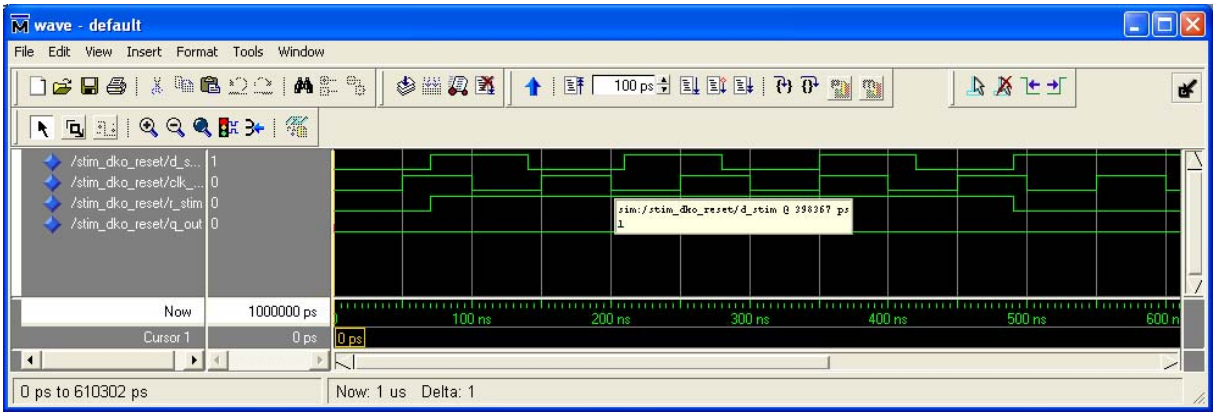
Funkčná imulácia:



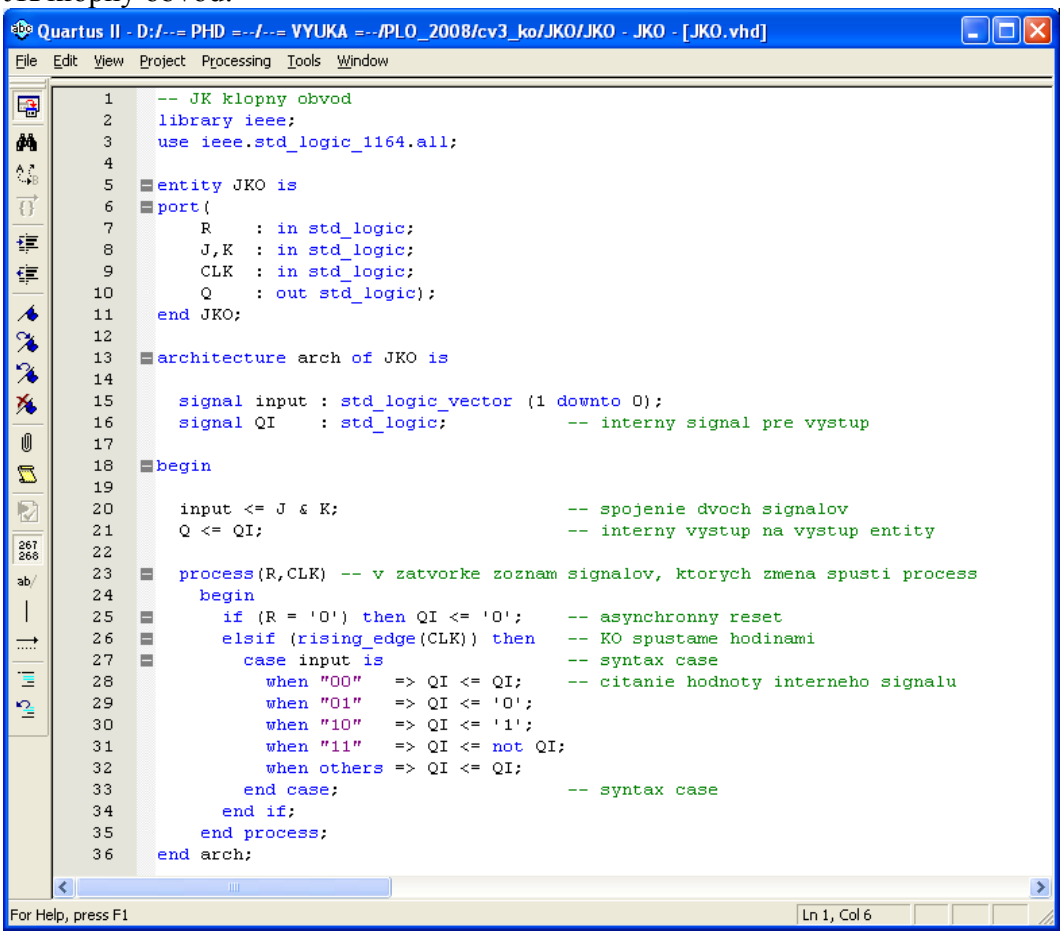
D klopný obvod s asynchrónnym resetom:



Funkčná simulácia



JK klopný obvod:



Funkčná simulácia: