Nástroje pre efektívny návrh FPGA aplikácií

Cieľ prednášky

Predstaviť prehľad nástrojov umožňujúcich návrh a realizáciu zložitých aplikácií na báze FPGA obvodov so zameraním na vložené (Embedded) aplikácie a číslicové spracovanie signálov (Digital Signal Processing).

Obsah

- LPM funkcie,
- MegaFunkcie/IP funkcie,
- MegacoreWizard,
- SOPC Builder,
- DSP Builder,
- FPGA a simulačné nástroje (Matlab, Simulink, Modelsim),
- NIOS II IDE.

Budú opisované riešenia pre obvody Altera, podobnú podporu poskytujú aj iní výrobcovia FPGA obvodov, IP funkcií a simulačných nástrojov.

LPM funkcie (Library of Parameterized Modules)

Problém:
- veľký nárast hustoty (FPGA) obvodov, výkonnosti, nových vlastností
- zachovanie nezávislosti návrhu od cieľového (FPGA) obvodu pri zachovaní efektívnosti (rýchlosť riešenia, doba implementácie, ...) riešenia

Riešenie (začiatok 90-tych rokov):
- definícia množiny štandardných funkcii podporované EDA (Electronic Design Automation) nástrojmi od rôznych výrobcova tiež výrobcami integrovaných obvodov
- LPM boli akceptované ako EIA (Electronic Industries Association) štandard v roku 1993

LPM je rozšírením EDIF (Electronic Design Interface Format), ktorý definuje syntax na prenos návrhov medzi nástrojmi od rôznych výrobcov EDA nástrojov.
LPM poskytuje knižnicu logických funkcii a modulov, ktoré sú nezávislé na cieľovej architektúre. LPM je parametrizovateľná knižnica umožňujúca ľahkú škálovateľnost a adaptáciu jednotllivých prvkov.

LPM Features

The primary objective for the LPM is to enable architecture-independent design without sacrificing efficiency. The LPM meets the following key criteria:

- *Architecture-independent design entry*—Designers can work with LPM functions during design entry and verification without specifying the target architecture. Design entry and simulation tools remain architecture-independent, relying on the synthesis or fitting tools to efficiently map the design to various architectures.
- *Efficient design mapping*—The LPM allows designers to create architecture-independent designs without sacrificing efficiency. The IC vendor is responsible for the mapping of LPM functions; thus, optimum solutions are guaranteed.
- *Tool-independent design entry*—The LPM enables designers to migrate designs between EDA tools while maintaining a high-level logic description of the functions. For example, designers can use one vendor's tool for logic synthesis and another vendor's tool for logic simulation.
- *Specification of a complete design*—LPM functions completely specify the digital logic for any design. Designers can create new functions with LPM functions.

Príklad Altera LPM funkcii (26 funkcií v roku 1996)

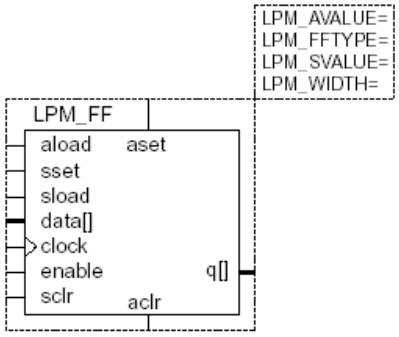
Table 1. LPM Functions

Type	Function	Description
Gates	lpm_and	Parameterized AND gate
	lpm_bustri	Parameterized tri-state buffer
	lpm_clshift	Parameterized combinatorial logic shifter or barrel shifter
	lpm_constant	Parameterized constant generator
	lpm_decode	Parameterized decoder
	lpm_inv	Parameterized inverter
	lpm_mux	Parameterized multiplexer
	lpm_or	Parameterized OR gate
	lpm_xor	Parameterized XOR gate
Arithmetic Components	lpm_abs	Parameterized absolute value megafunction
	lpm_add_sub	Parameterized adder/subtractor
	lpm_compare	Parameterized comparator
	lpm_counter	Parameterized counter
	lpm_mult	Parameterized multiplier
Storage Components	lpm_dff	Parameterized D-type flipflop and shift register
	lpm_ff	Parameterized flipflop
	lpm_latch	Parameterized latch
	lpm_ram_dq	Parameterized RAM with separate input and output ports
	lpm_ram_io	Parameterized RAM with a single I/O port
	lpm_rom	Parameterized ROM
	lpm_shiftreg	Parameterized shift register
	lpm_tff	Parameterized T-type flipflop

Príklad LPM funkcie klopného obvodu

lpm_ff

Parameterized D or T Flipflop



Ports

Name	Type	Required	Description
aload	Input	No	Asynchronous load input. Asynchronously loads the flipflop with the value on the data[] input. Default = 0. If aload is used, data[] must be used.
sset	Input	No	Synchronous set input. Sets the q[] outputs to the value specified by LPM_SVALUE, if that value is present, or sets the q[] outputs to all 1s. If both sset and sclr are used and both are asserted, sclr is dominant. The sset input affects the output q[] values before polarity is applied to the ports.
sload	Input	No	Synchronous load input. Loads the flipflop with the value on the data[] input on the next active clock edge. Default = 0. If sload is used, data[] must be used. For load operation, sload must be high (1) and enable must be high (1) or unconnected.
data[]	Input	No	T flipflop: toggle enable; D flipflop: data input. This port is LPM_WIDTH wide. If the data[] port is not used, at least one of the aset, aclr, sset, or sclr ports must be used.
clock	Input	Yes	Positive-edge-triggered clock.
enable	Input	No	Clock enable input. Default = 1.
sclr	Input	No	Synchronous clear input. If both sset and sclr are used and both are asserted, sclr is dominant. The sclr input affects the output q[] values before polarity is applied to the ports.
aset	Input	No	Asynchronous set input. Sets q[] outputs to the value specified by LPM_AVALUE, if that value is present, or sets the q[] outputs to all 1s.
aclr	Input	No	Asynchronous clear input. If both aset and aclr are used and both are asserted, aclr is dominant. The aclr input affects the output q[] values before polarity is applied to the ports.
q[]	Output	Yes	Data output from D flipflops. This port is LPM_WIDTH wide.

LPM Quick Reference Guide (1996)- ďalšie LPM funkcie

- http://www.altera.com/literature/catalogs/lpm.pdf
- Quartus II on-line manual

Príklad využitia LPM funkcie D – klopného obvodu

VHDL: Instantiating a D Flipflop using lpm_dff

This example instantiates an 8-bit-wide `D` flipflop using the `lpm_dff` function. The Port Map maps the pins in this instance of the function to the correspnding ports in the Component Instantiation Statement for the `lpm_dff` function, which is contained in the `lpm_component` package.

testdff.vhd

```
LIBRARY ieee, lpm;
USE ieee.std_logic_1164.ALL;
USE lpm.lpm_components.ALL;

ENTITY testdff IS
    PORT (inputs : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
          clk  : IN STD_LOGIC;
          aset : IN STD_LOGIC ;
          aclr : IN STD_LOGIC ;
          sset : IN STD_LOGIC ;
          sclr : IN STD_LOGIC ;
          en   : IN STD_LOGIC ;
          outputs : OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
END testdff;

ARCHITECTURE dff8 OF testdff IS
BEGIN
    U1 : lpm_ff
            GENERIC MAP(lpm_width => 8)
                PORT MAP(data => inputs,
                clock => clk,q => outputs,
                aclr => aclr, enable => en,
                aset => aset, sset => sset,
                sclr => sclr);
END;
```

Megafunkcie / IP funkcie

Megafunctions **are ready-made**, **parameterized, pre-tested blocks** of **intellectual property** that are optimized to make efficient use of the architecture of the targeted programmable device. By using megafunctions, designers can focus more time and energy on improving and differentiating their system-level product, rather than redesigning common functions. Megafunctions are supported in any complex programmable logic device (CPLD) design methodology, including existing hardware description language (HDL) design. When implementing complex system architectures, using megafunctions dramatically shortens design time, by allowing the reuse of existing intellectual property. Megafunctions provide total solutions by targeting specific application areas, providing optimized performance, significantly increasing design productivity and reducing time-to-market.

Zdroje (Altera) Megafunkcií

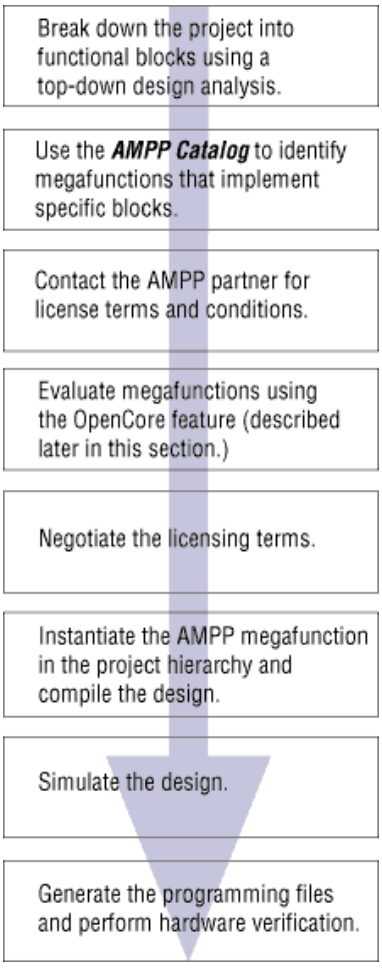
- Megafunctions from the Altera Megafunction Partners Program (AMPP^{SM})
- Megafunctions created by Altera, known as MegaCore functions
- Altera megafunction reference designs

AMPP Functions

The AMPP alliance between Altera and developers of intellectual property brings to users of Altera PLDs a wide range of synthesizable megafunctions that are optimized for Altera devices. A full listing of AMPP partners can be found on this web site. To obtain AMPP megafunctions, contact the vendor directly.

AMPP megafunctions are optimized for specific Altera device architectures. This optimization process usually involves setting compilation and synthesis options that maximize density and performance. AMPP megafunctions are then fine-tuned until they are as fast and small as possible.

Typický proces testovania, licencovania a použitia AMPP megafunkcií



Altera MegaCore Functions

Altera$^{Â®}$ MegaCore functions are developed and pre-tested by Altera and are optimized for specific Altera device architectures, allowing user-specified performance utilization goals to be met. These functions are licensed by Altera as MAX+PLUS II migration products. MegaCore functions can be downloaded from this web site.

Altera Intellectual Property: IP MegaStore

Get to Market Fast: Use IP MegaFunctions

IP MegaFunctions	Systems Integration & Tools Support	Partners
• Embedded Processor • Interface & Peripherals • DSP • Communication	• Quartus II • SOPC Builder • DSP Builder • Atlantic Interface • Nios II IDE • Development Kits	• AMPP IP • AMPP Software • ACAP Services • Embedded Software • EDA Partners
About IP	**IP Certifications**	**Documentation & Learning**
• Designing with IP • Free IP Evaluation • Licensing IP • Download IP	• SOPC Builder Ready • DSP Builder Ready • Atlantic Compliant • I-Tested • AMPP Approved	• Nios II Literature • MegaCore IP User Guides • Net Seminars

Altera Intellectual Property Design Flow

- inštalácia z CD alebo stiahnutie z www stránky
- **parametrizácia**
- testovanie s využitím **štandardných EDA** nástrojov
- testovanie v **cieľovom** hardv.
- **zakúpenie** megafunkcia

Reference Designs

Altera also provides free reference designs to help designers start the implementation process. Reference designs may include source code that can be easily modified to fit a designer's specific requirements. Reference designs for a variety of megafunctions are available.

Embedded Processors

Altera's intellectual property (IP) portfolio includes megafunctions that support Altera's embedded processor solutions.

The Nios II family of embedded processors offers user-configurable, general-purpose RISC processors and an easy-to-use development environment. The cost-effectiveness and flexibility of the Nios and Nios II processors has helped them to become among the most popular embedded processor architectures in the world, with many thousands of licensed users. The Nios II processor is available in several powerful development kits, and includes a library of standard peripherals.

Altera's IP portfolio provides many SOPC Builder-ready megafunctions that support the Nios II family of embedded processors. These cores also feature support for the Avalonâ„¢ switch fabric and the AHB interface, for quick and easy integration.

In addition to various other 32-bit processor architectures, the Altera IP portfolio includes 16- and 8-bit microcontroller solutions to address general co-processing requirements.

Megafunction Name *Vendor*	**PDF**	**Free Evaluation**	**Certifications**	
Nios II Embedded Processor *Altera Corporation*			SOPC Builder Ready	Stratix, Cyclone, Stratix II
Nios Soft Core Embedded Processor *Altera Corporation*			SOPC Builder Ready	Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, ACEX 1K, FLEX 10KE
2901 Four-Bit Microprocessor Slice *CAST, Inc.*		Try OpenCore	AMPP Approved, DSP Builder Ready	FLEX 10KE, ACEX 1K, APEX 20KE, Stratix, Cyclone, Stratix II
29116A 16-Bit Microprocessor *CAST, Inc.*		Try OpenCore	AMPP Approved, DSP Builder Ready	FLEX 10KE, ACEX 1K, APEX 20KE, Stratix, Stratix II
8-bit Microcontroller, 8051 *CAST, Inc.*		Try OpenCore	AMPP Approved, DSP Builder Ready	Stratix II, Cyclone, Stratix, APEX II, Excalibur, APEX 20KE, APEX 20KC, ACEX 1K, FLEX 10KE
C165X RISC Microcontroller *CAST, Inc.*		Try OpenCore	AMPP Approved, DSP Builder Ready	Stratix II, Stratix, APEX II, Excalibur, APEX 20KE, APEX 20KC, ACEX 1K, FLEX 10KE
C68000 Microprocessor *CAST, Inc.*		Try OpenCore	AMPP Approved, DSP Builder Ready	FLEX 10KE, APEX 20KE, APEX 20KC, APEX II, Stratix, Cyclone, Stratix II
CZ80CPU Processor *CAST, Inc.*		Try OpenCore	AMPP Approved, DSP Builder Ready	FLEX 10KE, ACEX 1K, Stratix, Stratix II

D80530 Microcontroller *CAST, Inc.*		Try OpenCore	AMPP Approved, DSP Builder Ready	Stratix II, Cyclone, Stratix, APEX II, Excalibur, APEX 20KE, APEX 20KC, ACEX 1K, FLEX 10KE
R8051 Microcontroller *CAST, Inc.*		Try OpenCore	AMPP Approved, DSP Builder Ready	Stratix II, Cyclone, Stratix, Excalibur, APEX 20KE, APEX 20KC, ACEX 1K, FLEX 10KE

Reference Designs *Vendor*	PDF	Download	IP Used	End Market	Device Support
Automotive Graphics System Reference Design *Altera Corporation*				Automotive	Cyclone II, Cyclone
Avalon Microsequencer Reference Design *Altera Corporation*		*Download*	SOPC Builder	Networking, Access & Transmission, Wireless, Computer, Storage, Industrial, Automotive	Cyclone II, Stratix II, Cyclone, Stratix
Avalon State Sequencer Reference Design *Altera Corporation*		*Download*	SOPC Builder	Networking, Access & Transmission, Wireless, Computer, Storage, Industrial, Automotive	Cyclone II, Stratix II, Cyclone, Stratix
Checksum Implemented with SOPC Builder Reference Design *Altera Corporation*			SOPC Builder	Networking, Access & Transmission, Wireless, Computer, Storage, Industrial, Automotive	Cyclone II, Stratix II, Cyclone, Stratix
CRC Hardware Acceleration Reference Design *Altera Corporation*		*Download*	Nios Soft Core Embedded Processor	Networking, Access & Transmission, Wireless, Computer, Storage, Industrial, Automotive	Stratix II, Stratix

Interfaces & Peripherals

Microsystems intellectual property (IP) functions from Altera provide system-on-a-programmable-chip (SOPC) integration, offering flexible peripherals, and supporting a wide variety of standard bus interfaces.

Designers can choose from Altera's comprehensive library of peripheral functions such as integrated design environments (IDEs), UARTs, interrupt controllers, and PCI bus bridges to build a custom function optimized for specific applications.

Altera's rapidly growing portfolio of standard bus interfaces allows users to add chip-to-chip, board-to-board, or box-to-box connectivity to SOPC designs. The microsystems portfolio also includes megafunctions to seamlessly add external memory, Ethernet interfaces, PCI, PCI-X, universal serial bus (USB), and next-generation processor interfaces.

Megafunction Name *Vendor*	PDF	Free Evaluation	Certifications	
DDR SDRAM Controller *Altera Corporation*		Try OpenCore Plus	SOPC Builder Ready, I-Tested	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX
DDR2 SDRAM Controller *Altera Corporation*		Try OpenCore Plus	SOPC Builder Ready, I-Tested	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX
HyperTransport *Altera Corporation*		Try OpenCore Plus	Atlantic Compliant, I-Tested	Stratix, Stratix GX, Stratix II
Parallel & Serial RapidIO Physical Layer *Altera Corporation*		Try OpenCore Plus	Atlantic Compliant, I-Tested	Stratix II, Stratix, Stratix GX
PCI Compiler, 32-bit Master/Target *Altera Corporation*		Try OpenCore Plus	I-Tested	Cyclone II, MAX II, Stratix II, Cyclone, Stratix, Stratix GX
PCI Compiler, 32-bit Target *Altera Corporation*		Try OpenCore Plus	I-Tested	Cyclone II, MAX II, Stratix II, Cyclone, Stratix, Stratix GX
PCI Compiler, 64-bit Master/Target *Altera Corporation*		Try OpenCore Plus	I-Tested	Cyclone II, MAX II, Stratix II, Cyclone, Stratix, Stratix GX
PCI Compiler, 64-bit Target *Altera Corporation*		Try OpenCore Plus	I-Tested	Cyclone II, MAX II, Stratix II, Cyclone, Stratix, Stratix GX
PCI32 Nios Target *Altera Corporation*		Try OpenCore	SOPC Builder Ready, I-Tested	Cyclone, Stratix, Stratix GX, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K, ACEX 1K, FLEX 10KE

QDRII SRAM Controller *Altera Corporation*		Try OpenCore Plus	I-Tested	Cyclone II, Stratix II, Stratix, Stratix GX

Reference Designs *Vendor*	PDF	Download	IP Used	End Market	Device Support
AES3/EBU Reference Design *Altera Corporation*				Broadcast	Cyclone II, Cyclone, Stratix, Stratix GX
Asynchronous Serial Interface (ASI) Implementation for MPEG-2 Video Reference Design *Altera Corporation*				Broadcast	Cyclone II, Cyclone, Stratix, Stratix GX
Bridge from FT425BM to Nios Avalon Bus Reference Design *Altera Corporation*				Computing	Cyclone II, Cyclone
CPRI Reference Design *Altera Corporation*				Wireless	Stratix GX
FPGA Design Security Using MAX II *Altera Corporation*				Networking, Access & Transmission, Wireless, Computer, Storage, Industrial, Automotive	Stratix II GX, Cyclone II, MAX II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K, ACEX 1K, FLEX 10KE, FLEX 6K
High-Speed Interface for Fujitsu MB86064 DACs Reference Design *Altera Corporation*		*Download*		Wireless	Stratix II, Stratix
I2C Controller Reference Design *Altera Corporation*		*Download*		Industrial, Automotive, Computer, Other	Cyclone II, MAX II, Stratix II, Cyclone, Stratix
Link-Port Reference Design *Altera Corporation*		*Download*		Wireless	Cyclone II, Stratix II, Cyclone, Stratix
OBSAI RP3 Reference Design				Wireless	Stratix GX

Altera Corporation					
SDR SDRAM Controller Reference Design *Altera Corporation*		*Download*		Networking, Access & Transmission, Wireless, Computer, Storage, Industrial, Automotive	Cyclone, Stratix

DSP

Altera's digital signal processing (DSP) portfolio consists of proven, high-performance, standard algorithms and functions created to help engineers meet today's rapidly evolving technologies. Each MegaCore and AMPP function has been rigorously tested and meets the exacting requirements of various industry standards.

Altera® provides an extensive portfolio of drop-in DSP functions. The DSP portfolio includes everything you need to build system-on-a-programmable-chip (SOPC) solutions. You can choose blocks of intellectual property (IP) from our comprehensive range of standard DSP functions to create a complete SOPC solution. And because these functions are reusable, you can instantiate each function multiple times in different designs.

DSP algorithms can be integrated easily as hardware accelerators for a Nios II processor or into the data path as a pre- or post-processor to implement computationally rigorous routines, leaving the digital signal processor at the center of the original design. Adding a high-performance FPGA to address bottlenecks at both ends of a process allows DSP software engineers to leverage existing software code while enjoying the benefits of hardware acceleration.

Megafunction Name *Vendor*	**PDF**	**Free Evaluation**	**Certifications**	
Color Space Converter *Altera Corporation*		Try OpenCore Plus	DSP Builder Ready	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, APEX 20KE, APEX 20KC, ACEX 1K, FLEX 10KE
FFT/IFFT *Altera Corporation*		Try OpenCore Plus	DSP Builder Ready, Atlantic Compliant	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX
FIR Compiler *Altera Corporation*		Try OpenCore Plus	DSP Builder Ready, Atlantic Compliant	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX
Numerically Controlled Oscillator Compiler *Altera Corporation*		Try OpenCore Plus	DSP Builder Ready	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K, ACEX 1K, FLEX 10KE
Reed-Solomon Compiler, Decoder *Altera Corporation*		Try OpenCore Plus	DSP Builder Ready	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K, ACEX 1K, FLEX 10KE

Reed-Solomon Compiler, Encoder *Altera Corporation*		Try OpenCore Plus	DSP Builder Ready	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K, ACEX 1K, FLEX 10KE
Turbo Decoder Function *Altera Corporation*		Try OpenCore Plus		Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K
Turbo Encoder Function *Altera Corporation*		Try OpenCore Plus		Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K
Viterbi Compiler, High-Speed Parallel Decoder *Altera Corporation*		Try OpenCore Plus	DSP Builder Ready, Atlantic Compliant	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K, ACEX 1K, FLEX 10KE
Viterbi Compiler, Low-Speed/Hybrid Serial Decoder *Altera Corporation*		Try OpenCore Plus	DSP Builder Ready, Atlantic Compliant	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K, ACEX 1K, FLEX 10KE

Reference Designs *Vendor*	PDF	Download	IP Used	End Market	Device Support
CORDIC Reference Design *Altera Corporation*				Wireless	Cyclone, Stratix
Digital Predistortion Reference Design *Altera Corporation*			Nios Soft Core Embedded Processor	Wireless	Stratix II, Stratix
Edge Detection Reference Design *Altera Corporation*		*Download*	DSP Builder, DSP Development Kit Stratix II Edition , SOPC Builder	Industrial	Stratix II
EMIF Co-Processor Reference Design *Altera Corporation*		*Download*	FFT/IFFT	Wireless	Stratix II
Floating Point FFT *Altera Corporation*				Networking, Access & Transmission, Wireless	Stratix, Stratix GX
Gold Code Generator Reference Design *Altera Corporation*		*Download*	SOPC Builder, Nios Soft Core Embedded Processor	Wireless	APEX 20K

Quadrature Phase Shift Keying Reference Design *Altera Corporation*			Numerically Controlled Oscillator Compiler, Reed-Solomon Compiler Decoder, Reed-Solomon Compiler Encoder, Viterbi Compiler High-Speed Parallel Decoder	Networking, Access & Transmission, Wireless	Stratix
Turbo Encoder Co-processor Reference Design *Altera Corporation*			Turbo Encoder Function	Wireless	Cyclone II, Stratix II, Cyclone, Stratix

Communications

Altera communications intellectual property (IP) megafunctions provide complex, standards-based cores that can be combined with user-designed logic to develop unique solutions in a single device. The Altera communications portfolio for telecom and datacom consists of core functions for Ethernet, cell/packet, SONET/SDH, and T/E carrier networking infrastructures, as well as high-speed interfaces for UTOPIA, POS-PHY, system packet interface, and backplane use. These megafunctions are ideal for high-performance DSLAMs, access concentrators, edge routers, multiplexers, and multiservice switches, and their integration and flexibility benefits enable a comprehensive system-on-a-programmable-chip (SOPC) solution.

Megafunction Name *Vendor*	PDF	Free Evaluation	Certifications	
8B10B Encoder/Decoder *Altera Corporation*		Try OpenCore Plus		Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, APEX 20KE, APEX 20KC
POS-PHY Level 2 Link *Altera Corporation*		Try OpenCore Plus	Atlantic Compliant	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K
POS-PHY Level 2 PHY *Altera Corporation*		Try OpenCore Plus	Atlantic Compliant	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K
POS-PHY Level 3 Link *Altera Corporation*		Try OpenCore Plus	Atlantic Compliant	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K
POS-PHY Level 3 PHY *Altera Corporation*		Try OpenCore Plus	Atlantic Compliant	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K
POS-PHY Level 4 *Altera Corporation*		Try OpenCore Plus	Atlantic Compliant, I-Tested	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX
SONET/SDH Compiler *Altera Corporation*		Try OpenCore Plus	I-Tested	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX

UTOPIA Level 2 Master *Altera Corporation*		Try OpenCore Plus	Atlantic Compliant, I-Tested	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K, ACEX 1K, FLEX 10KE
UTOPIA Level 2 Slave *Altera Corporation*		Try OpenCore Plus	Atlantic Compliant, I-Tested	Cyclone II, Stratix II, Cyclone, Stratix, Stratix GX, Mercury, APEX II, Excalibur, APEX 20KE, APEX 20KC, APEX 20K, ACEX 1K, FLEX 10KE
ATM Deformatter *Adaptive Micro-Ware*		Try OpenCore	AMPP Approved	ACEX 1K, APEX 20KE, Stratix, Stratix II, Cyclone

Reference Designs *Vendor*	PDF	Download	IP Used	End Market	Device Support
Media Independent Interface (MII) Reference Design *Altera Corporation*			Nios Soft Core Embedded Processor	Networking, Access & Transmission	Stratix II, Stratix
SPI-4.2 Universal SmartBridge Reference Design *Modelware*				Wireline, Networking, Access and Transmission	Stratix II, Stratix

Príklad referenčného návrhu - QPSK Modem Reference Design, Application Note 281, October 2003, ver. 2.1

Features

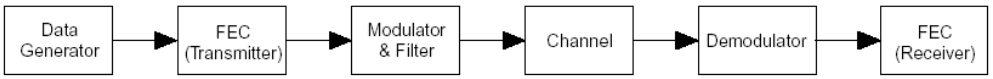
The QPSK modem reference design provides the following features:

- Single data channel at 5 Mbps
- Concatenated RS/Viterbi forward error correction
- 110 dB SFDR 20 MHz carrier
- 80 MSPS transmitter output with 10 MHz bandwidth and 20 dB out-of-band rejection

Functional Description

Figure 2 shows a simple block diagram for the QPSK modem reference design.

Figure 2. QPSK Modem Reference Block Diagram



The QPSK modem reference design is a basic design that uses a simplified channel model. It implements an encoder, a channel, and a decoder, and uses modulation, filtering, and error correction. It does not implement any synchronization functions. The parameters used in the design are arbitrary, and do not conform to any particular standard.

The design uses the following items:

- Stratix device DSP blocks
- Altera® Viterbi Compiler MegaCore® function
- Altera Reed-Solomon (RS) Compiler MegaCore function
- Altera numerically controlled oscillator (NCO) Compiler MegaCore function
- Altera FIR Compiler MegaCore function
- DSP Builder with the SignalTap® II logic analyzer read-back feature
- ModelSim PE or SE simulator
- Quartus® II software version 3.0
- MATLAB version 6.5 and Simulink version 5.1, including the DSP and communications blockset
- Stratix EP1S25 DSP development board or the Stratix EP1S80 DSP development board

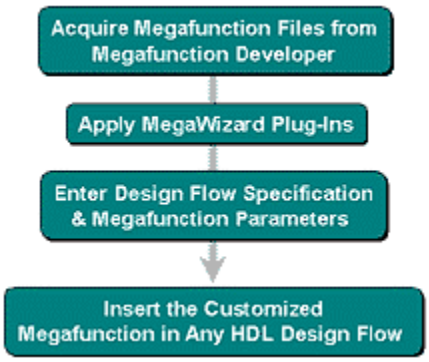
When you install the software from the *DSP Development Kit, Stratix Edition* CD-ROM, the design files are installed in the directory structure shown in Figure 1.

MegaWizard Plug-Ins

MegaWizard Plug-Ins are parameterization tools that help you integrate megafunctions into your designs without requiring the use of third-party tools. You can use this feature in the Quartus II and MAX+PLUS II (version 8.2 and higher) software or as a stand-alone tool with third-party EDA design interfaces. MegaWizard Plug-Ins provide maximum flexibility, allowing you to customize megafunctions without changing your design's source code. You can integrate a parameterized megafunction in any hardware description language (HDL) or netlist file using any EDA tool.

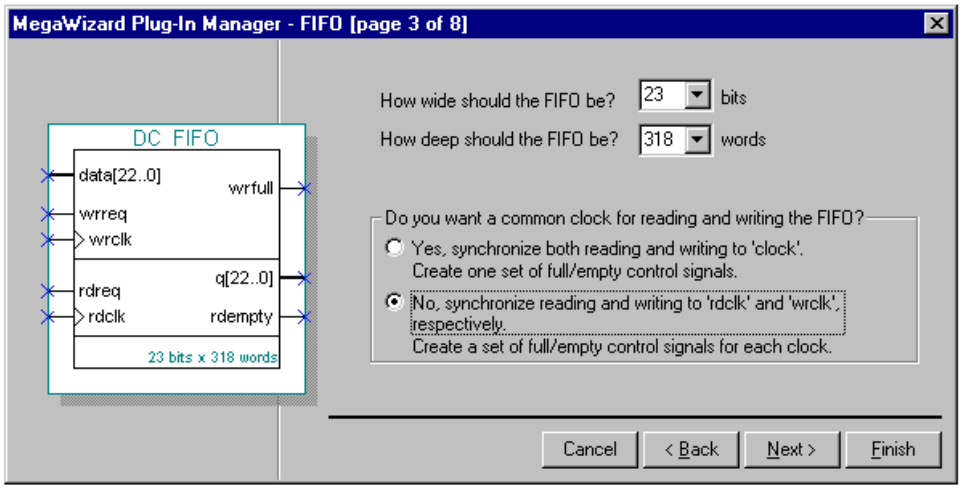
MegaWizard Plug-In Design Flow

The following diagram illustrates the design flow for using MegaWizard Plug-Ins with parameterized megafunctions.

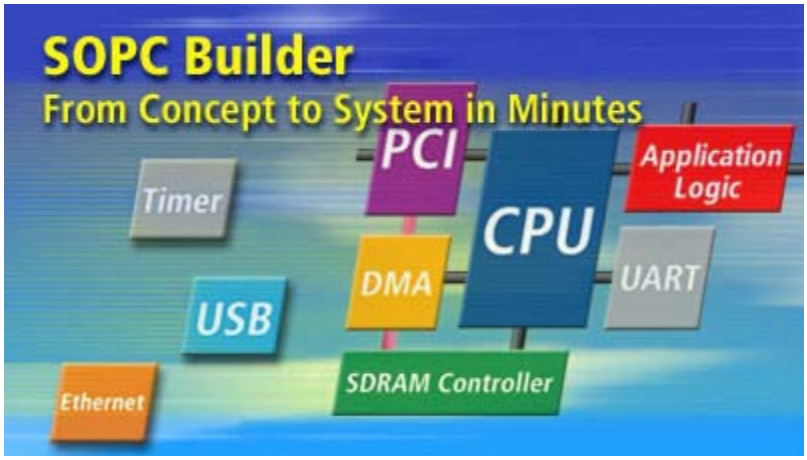


The Quartus II and MAX+PLUS II MegaWizard Plug-In Manager allows you to bring up the megafunction's wizard so that you can set the parameters of the megafunction to fit your design. A custom megafunction variation is then generated that you can instantiate in your design file.

Príklad konfigurácie FIFO megafunkcie v okne MegaWizardu:



SOPC (System on a Programmable Chip) Builder



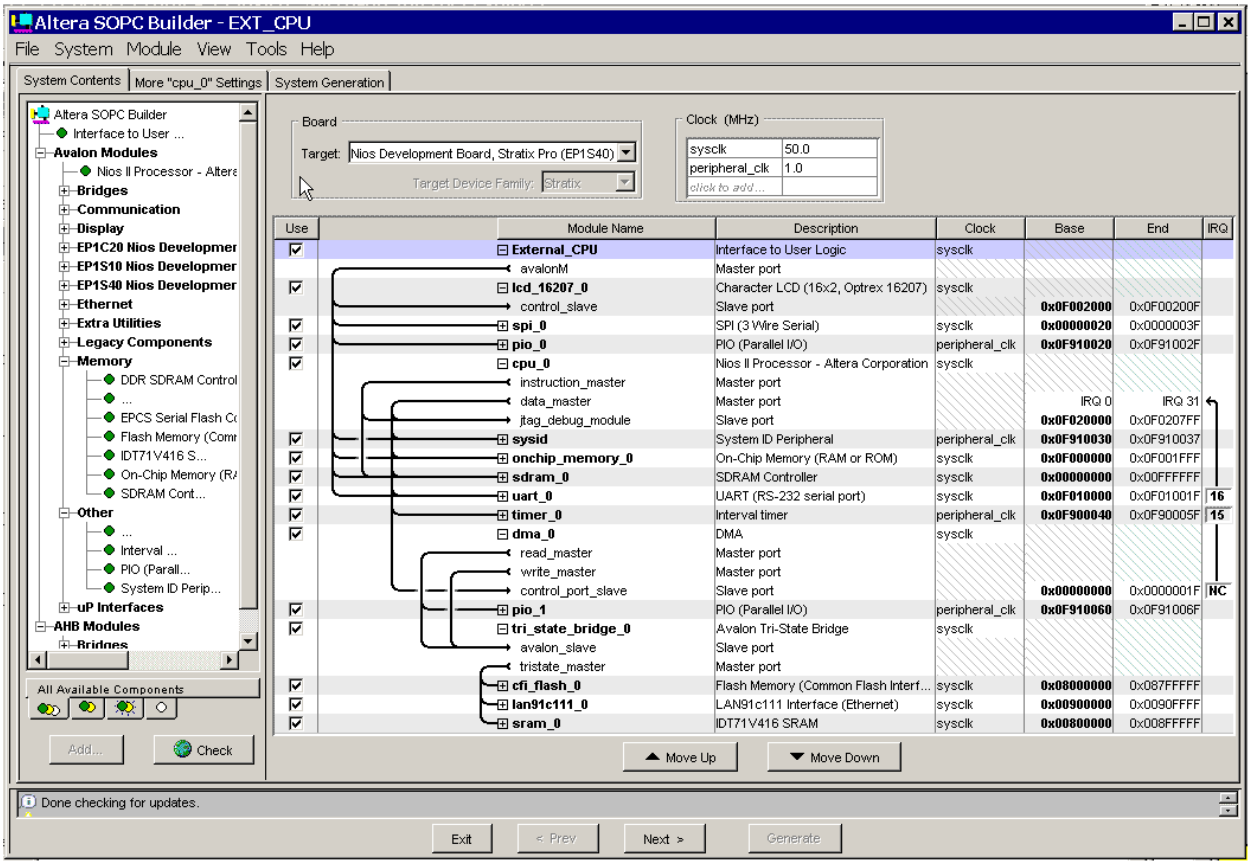
The SOPC Builder tool is a revolutionary system development tool that minimizes time spent integrating components. SOPC Builder enables rapid development of custom solutions and regeneration of existing solutions to add new capabilities and improve system performance. By automating the integration phase of system components, SOPC Builder allows users to focus attention on system-level requirements instead of the mundane, manual task of integrating components of varying requirements. All versions of the Altera Quartus II design software contain SOPC Builder.

SOPC Builder provides a powerful platform for composing systems defined at the block or component level. The SOPC Builder library of components range from simple blocks of fixed logic to complex, parameterized, and dynamically generated subsystems. These components can be purchased as intellectual property (IP) cores from Altera or from third parties, and some can be downloaded and evaluated for free. Users can also easily create their own custom SOPC Builder components. The SOPC Builder library of available components includes:

- Processors
  - On-Chip Processors
  - Interfaces to Off-Chip Processors
- IP & Peripherals
  - Memory Interfaces
  - Common Micro-Peripherals
  - Communications Peripherals
  - Bridges & Interfaces
  - Digital Signal Processing (DSP) IP
  - Hardware Accelerators Peripherals

Užívateľské rozhranie SOPC Buildera

SOPC Builder



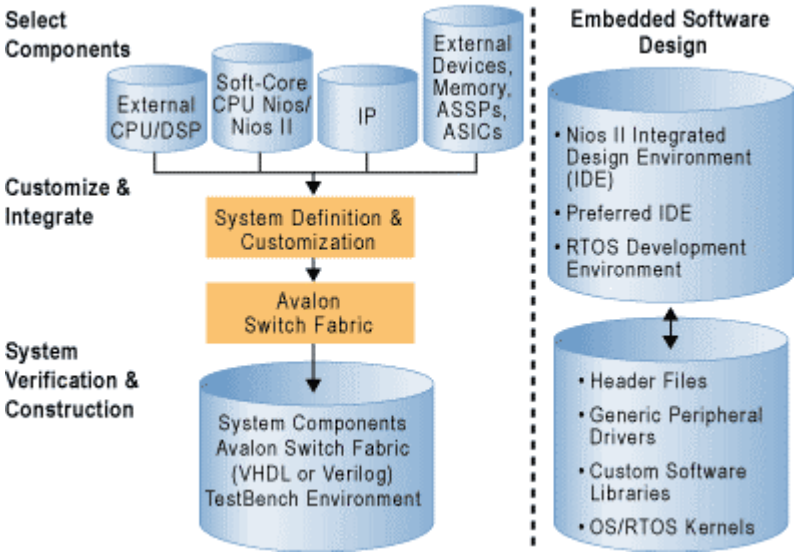
Výhody

SOPC Builder system design leverages the logic, memory, DSP blocks, and specialized I/O advantages of programmable logic devices (PLDs), including:

- Flexibility of logic capacity, memory and DSP blocks, and specialized I/O standards
- Fast time-to-market
- No non-recurring engineering (NRE) costs
- No fabrication or expensive design tools required
- Low risk - users can verify designs in silicon, at speed with real-world stimulus

SOPC Builder Design Flow

The SOPC Builder tool, included with the Quartus II design software, **automatically** generates the interconnect logic (Avalon switch fabric) connecting components used in SOPC applications. The components include **embedded processors** that are internal or external to the FPGA and **peripherals**, including **intellectual property** (IP) cores and **customer-created peripheral cores**, and off-chip devices such as ASSPs and ASICs. With the export of header files and peripheral drivers, SOPC Builder accelerates the development of application software. SOPC Builder enables designers to focus on the key components of their systems and begin developing the applications sooner by eliminating the engineering time required for system integration tasks.



DSP Builder

DSP Builder is a digital signal processing (DSP) development tool that interfaces between the Quartus II software and MATLAB/Simulink tools.

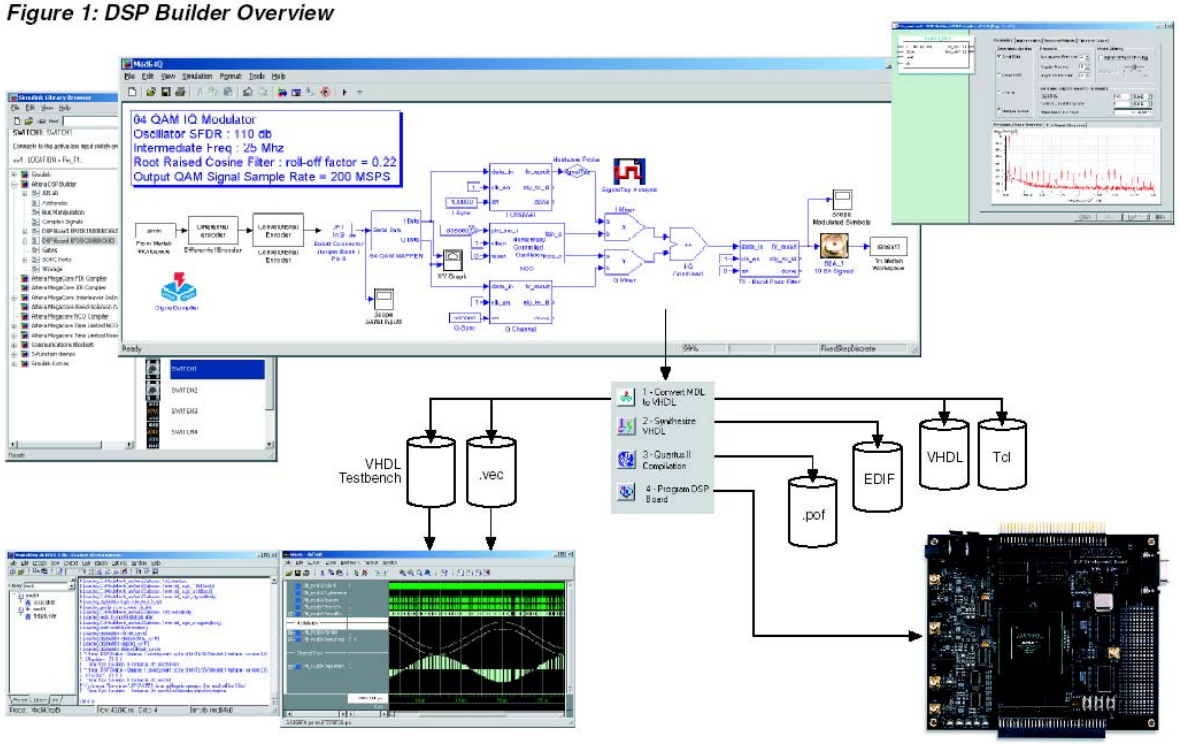
Vlastnosti

- Links The MathWorks MATLAB (Signal Processing Toolbox and Filter Design Toolbox) and Simulink software with the Altera Quartus II software
- Supports the latest Altera device families:
  - Stratix, Stratix II, and Stratix GX devices
  - Cyclone and Cyclone II devices
- Enables rapid prototyping using Altera DSP development boards
- Supports the SignalTap® II logic analyzer, an embedded signal analyzer that probes signals from the Altera device on the DSP board and imports the data into the MATLAB work space to facilitate visual analysis
- Includes blocks you can use to build custom logic that works with Nios II and other SOPC Builder designs
- Includes a phase-locked loop (PLL) block for multi-clock designs
- Includes a state machine block
- Supports a unified representation of the algorithm and implementation of a DSP system
- Automatically generates a VHDL testbench or Quartus II Vector File (.**vec**) from MATLAB and Simulink test vectors
- Automatically starts Quartus II compilation
- Enables bit- and cycle-accurate design simulation
- Provides a variety of fixed-point arithmetic and logical operators for use with the Simulink software

DSP system design in Altera programmable logic devices (PLDs) requires both high-level algorithm and hardware description language (HDL) development tools. The Altera DSP Builder integrates these tools by combining the algorithm development, simulation, and verification capabilities of The MathWorks MATLAB and Simulink system-level design tools with VHDL synthesis, simulation, and Altera development tools. The DSP Builder shortens DSP design cycles by helping designers create the hardware representation of a DSP design in an algorithm-friendly development environment. The existing MATLAB functions and Simulink blocks can be combined with Altera DSP Builder blocks and Altera intellectual property (IP) MegaCore® functions to link system-level design and implementation with DSP algorithm development. DSP Builder allows system, algorithm, and hardware designers to share a common development platform.

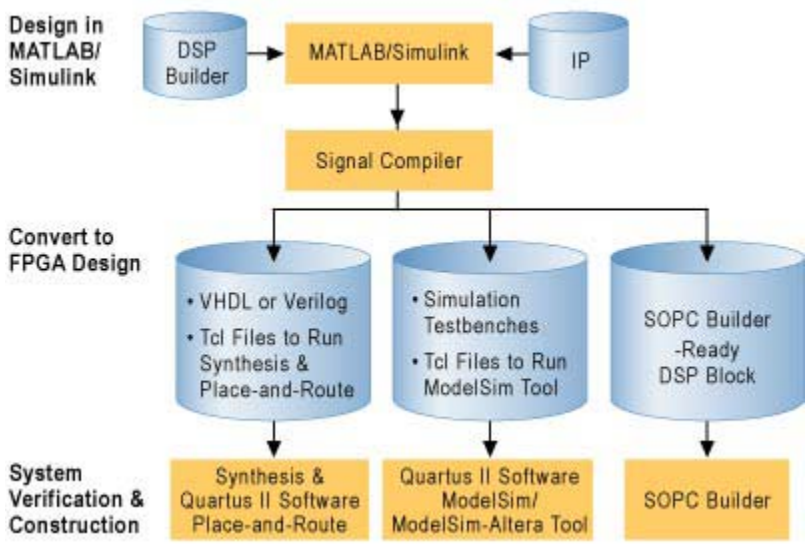
Designers can use the blocks in DSP Builder to create a hardware implementation of a system modeled in Simulink in sampled time. DSP Builder contains bit- and cycle-accurate Simulink blocks, which cover basic operations such as arithmetic or storage functions. Complex functions can be integrated by using MegaCore functions in DSP Builder models. See Figure 1.

Figure 1: DSP Builder Overview



DSP Builder Design Flow

Using Altera's DSP Builder, designers can perform **algorithmic digital signal processing (DSP) design at a high level of abstraction** in The MathWorks' MATLAB and Simulink software. They can then **push a button** to **port the design to hardware description language (HDL)** files. The DSP Builder can generate **SOPC Builder Ready DSP** blocks that can be easily integrated into a complete SOPC system design using the SOPC Builder. Figure 2 shows a high-level view of the DSP Builder design flow.



Hardware-Software Co-Simulation

Designers can use system-level design tools **for early-in-design testing** of hardware and software interactions through **testbench files and simulation models** before they construct any hardware prototypes. Designers can also use the **rapid system generation** and hardware-software **co-simulation** features to perform tradeoff analysis of which functions should be implemented in hardware versus embedded software.

Podrobnejšie informácie
DSP Builder User Guide (http://www.altera.com/literature/ug/ug_dsp_builder.pdf)
DSP Builder Reference Manual (http://www.altera.com/literature/manual/mnl_dsp_builder.pdf)

Nios II Integrated Development Environment

Poskytuje moderné integrované prostredie pre návrh vložených aplikácií na báze vloženého procesor Altera NIOS II.

The Nios II integrated development environment (IDE) is the primary software development tool for the Nios II family of embedded processors. All software development tasks can be accomplished within the Nios II IDE, including editing, building, and debugging programs. The Nios II IDE provides a consistent development platform that works for all Nios II processor systems. With a PC, an Altera FPGA, and a JTAG download cable, software developers have everything needed to write programs for, and communicate with, any Nios II processor system.

The Nios II IDE provides four main functions for software development:

- Project manager
- Editor and compiler
- Debugger
- Flash programmer

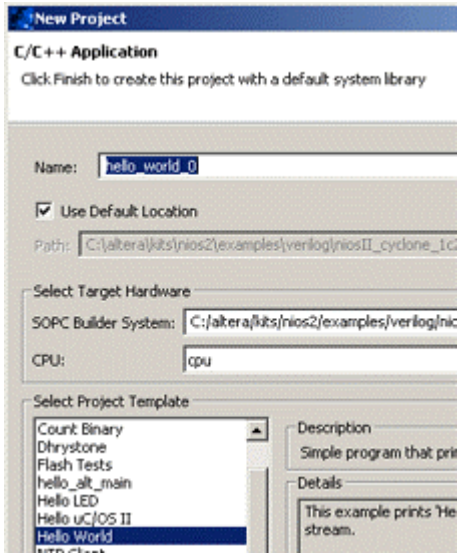
The Nios II IDE is based on the open, extensible Eclipse IDE project and the Eclipse C/C++ Development Tools (CDT) Project. Learn more about the Eclipse Project at http://www.eclipse.org/.

Project Manager

The Nios II IDE provides several project management tasks that speed up the development of embedded applications.

New Project Wizard - The Nios II IDE presents a new project wizard (shown in figure 1, below), used to automate the set-up of the C/C++ application project and system library projects. With the new project wizard, setting up new projects within the Nios II IDE is a snap.

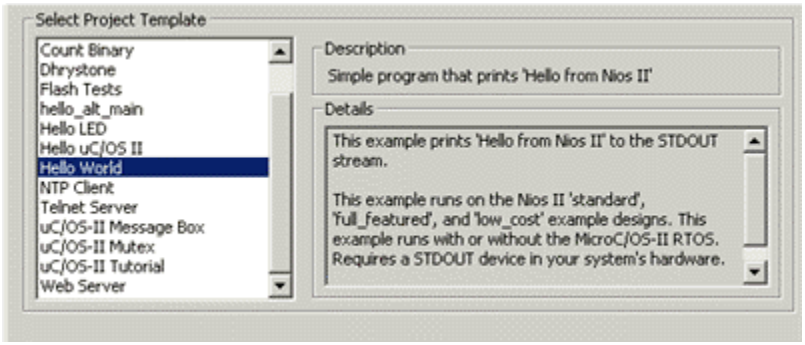
Figure 1. Nios II IDE New Project Wizard



Software Project Templates - In addition to a project set-up wizard, the Nios II IDE provides software code examples, in the form of project templates, to help software engineers bring up working systems as quickly as possible.

Each template is a collection of software files and project settings. Designers can add their own source code to the project by placing the code in the project directory or importing the files into the project. Figure 2 shows some of the available software project templates.

Figure 2. Software Project Templates



Software Components - The Nios II IDE lets designers customize systems quickly using software components. Software components (also referred to as "system software") provide designers with an easy way to painlessly configure their system for their specific target hardware.

Components included:

- Nios II run-time library (also known as the hardware abstraction layer (HAL))
- Lightweight IP TCP/IP stack
- MicroC/OS-II real-time operating system (RTOS)
- Altera Zip file system

To learn more check out the *Nios II Software Developer's Handbook*, as well as the *MicroC/OS-II RTOS tutorial*.

Editor and Compiler

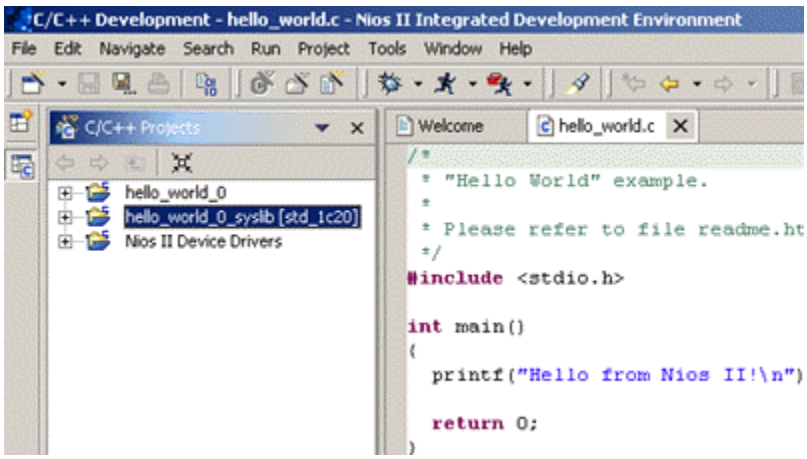
Altera's Nios II IDE provides a full-featured source editor and C/C++ compiler.

Text Editor - The Nios II IDE text editor is a mature, full-featured source editor. Some of the features include:

- Syntax highlighting - C/C++
- Code assist / code completion
- Comprehensive search facilities
- File management
- Extensive on-line help topics & tutorials
- Import assistance
- Quick fix, auto-corrections
- Integrated debugging features

Figure 3, below, shows a screen capture of the Nios II IDE text editor highlighting C source code.

Figure 3. Basic Editing Provided By the Nios II IDE



C/C++ Compiler - Based on the industry-standard GNU tool chain, the Nios II IDE provides a graphical user interface to the GCC compiler. The Nios II IDE build environment is designed to facilitate software development for Altera's Nios II processors, providing an easy-to-use push-button flow, while also allowing designers to manipulate advanced build settings.

The Nios II IDE build environment automatically produces a makefile based on the user's specific system configuration (the SOPC Builder-generated PTF file). Changes made in the Nios II IDE compiler/linker settings are automatically reflected in this auto-generated makefile. These settings can include options for the generation of memory initialization files (MIF), flash content, simulator initialization files (DAT/HEX), and profile summary files.

More information on the Nios II IDE C/C++ compiler and build environment is available in the *Nios II Software Developer's Handbook, Altera-Provided Development Tools* and the Nios II IDE online help.

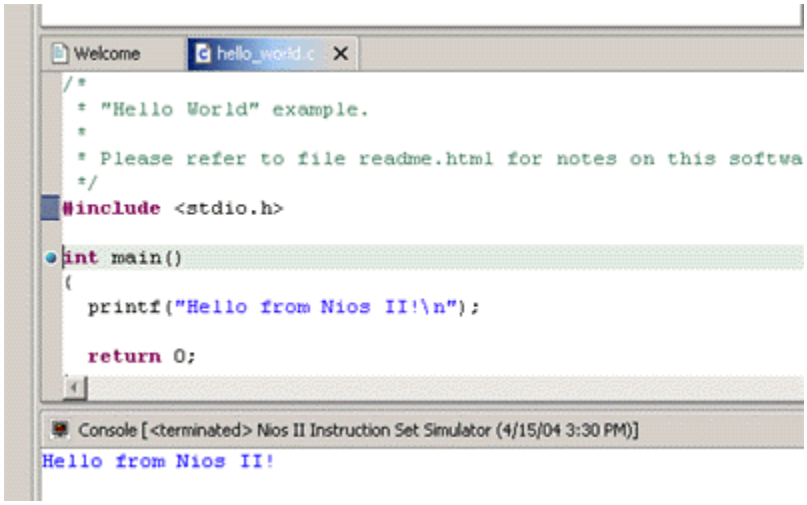
Debugger

The Nios II IDE contains a robust software debugger based on the GNU debugger, GDB. The debugger provides many basic debug features, as well as several advanced debug features not usually available with low-cost processor development kits.

Basic debug - The Nios II IDE debugger contains basic debug features such as:

- Run control
- Call stack view
- Software breakpoints
- Disassembly code view
- Debug information view
- Instruction set simulator (ISS) target

Figure 4. Nios II IDE Debugger Breakpoints



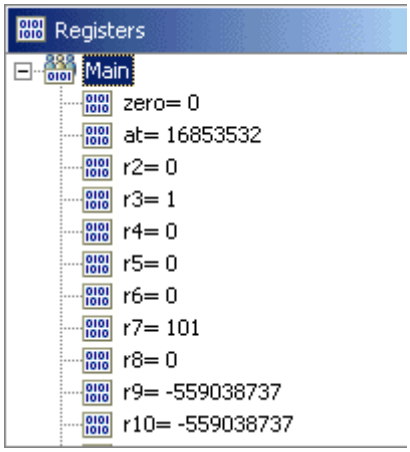
Advanced debug - In addition to the basic debug features outlined above, the Nios II IDE debugger also has several advanced debugging capabilities, such as:

- Hardware breakpoints for debugging code in ROM or flash
- Data triggers
- Instruction trace

The Nios II IDE debugger connects to the target hardware using a JTAG debug module. Additionally, support for off-chip trace is provided to work with 3rd party trace probes such as the in-target system analyzer for the Nios II processor (ISA-NIOS) from FS2.

Debug information view - The debug information view provides the users with access to local variables, registers, memory, breakpoints, and expression evaluation functions. Figure 5 shows an example of this debug information view, showing the register display of an example application.

Figure 5. Debug Information View - Register Display



Targets - The Nios II IDE debugger can connect to several targets types. Table 1 shows the available target connections within the Nios II IDE debugger.

Table 1. Nios II IDE Debugger Targets

Target	Description
Hardware (via JTAG)	Connect to Altera FPGA development board, such as those available in a Nios II development kit or other Altera or partner kits.
Instruction set simulator	Software implmentation of the Nios II instruction set architecture; used for system development before a hardware platform (e.g. FPGA circuit board) is available.
Hardware logic simulator	Connection to ModelSim HDL simulator; useful for systems with user-created peripherals that need to be verified.

Flash Programmer

Many designs that utilize Nios II processors also incorporate flash memory on the board as a means to store an FPGA configuration and/or Nios II program data. The Nios II IDE includes a convenient method of programming this flash. Any common flash interface (CFI) compliant flash device connected to the FPGA can be programmed using the Nios II IDE flash programmer. In addition to CFI flash, the Nios II IDE flash programmer can program any Altera serial configuration device connected to the FPGA.

The flash programmer manages several types of data, such as:

Table 2. Content Types Commonly Programmed Into Flash

Type of Content	Description
System firmware	Programming software into flash allows the Nios II processor to boot from flash upon reset
FPGA configuration	If using a configuration controller (such as that used on Nios development boards), the FPGA can be configured from flash upon power-on reset
Arbitrary binary data	Can be any type of binary data that the designer wishes to store into flash, such as graphics, audio, etc.

The Nios II IDE flash programmer features an easy-to-use interface (shown in figure 6, below).

Figure 6. Flash Programmer Interface