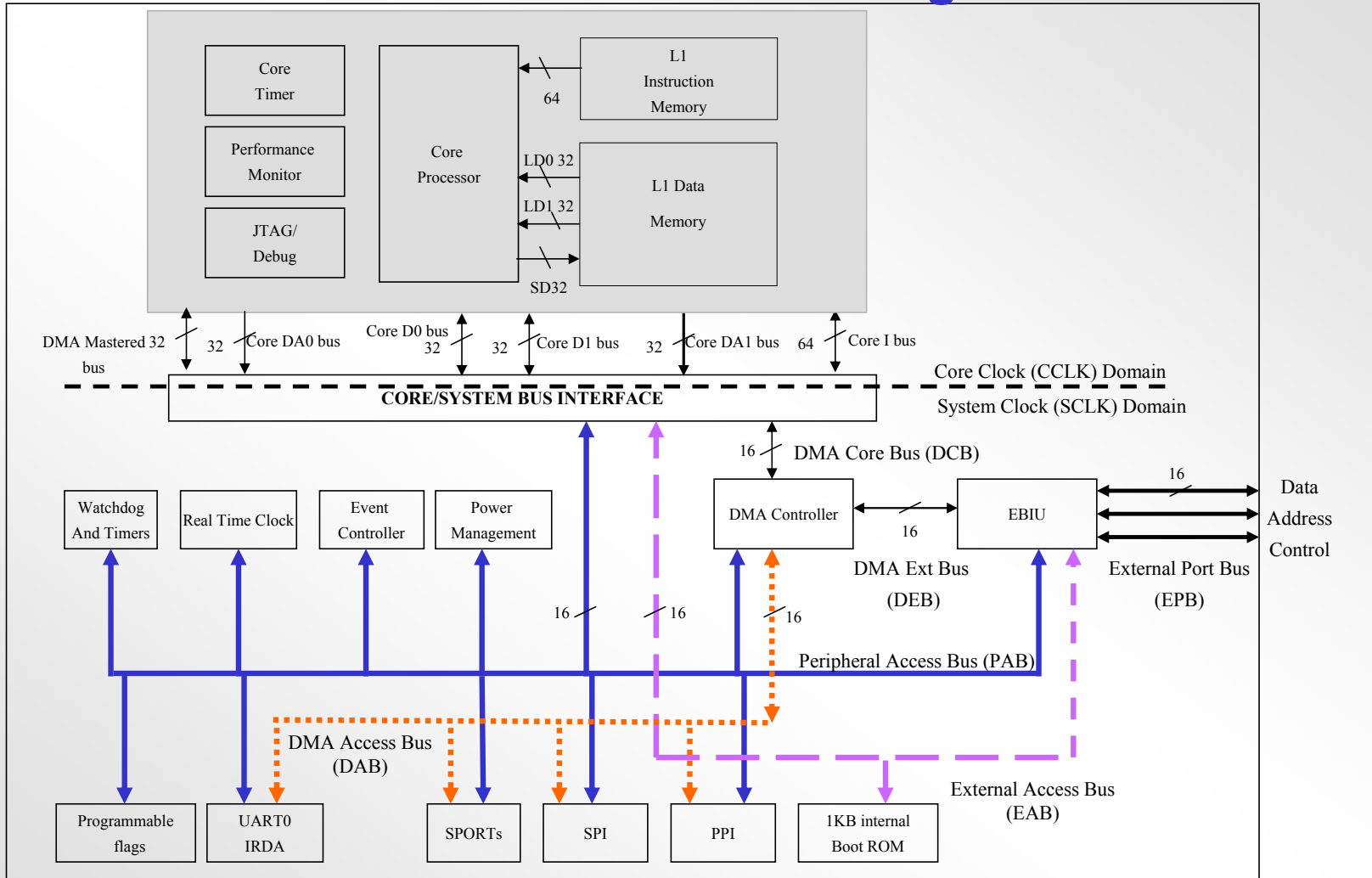


Section 14

Parallel Peripheral Interface (PPI)

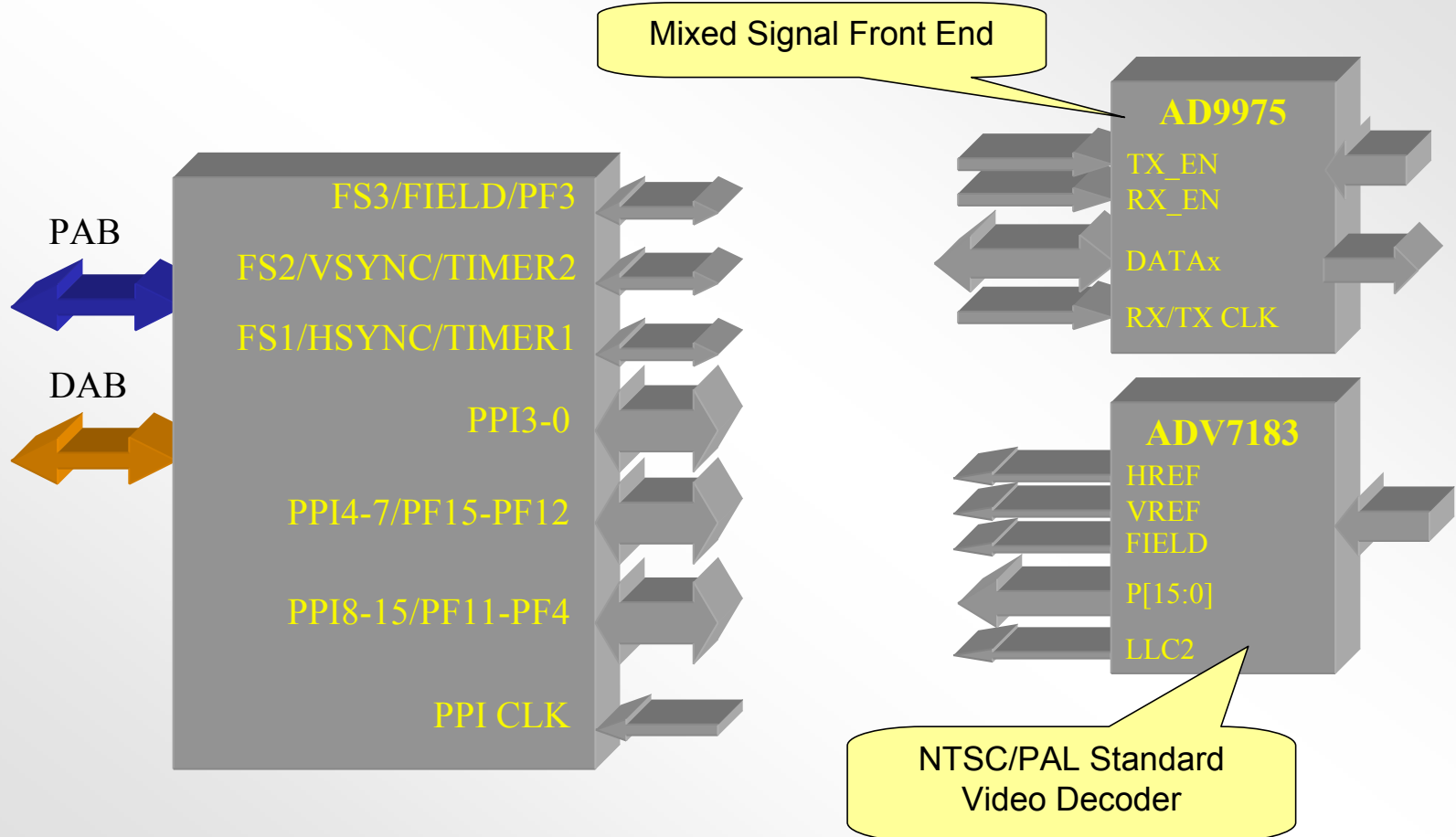
ADSP-BF533 Block Diagram



PPI - What is it?

- **Parallel Peripheral Interface**
 - Programmable bus width (from 8 – 16 bits in 1-bit steps)
 - Bidirectional (half-duplex) parallel interface
 - Synchronous Interface
 - Interface is driven by an external clock (“PPI_CLK”)
 - Up to 66MHz rate (SCLK/2)
 - Asynchronous to SCLK
 - Includes three frame syncs to control the interface timing
 - Applications
 - High speed data converters
 - Video CODECs
- **Used in conjunction with a DMA channel**
 - Can setup 2D DMA (e.g., for video)
 - Can pack 8-bit bytes into 16-bit words for efficient I/O

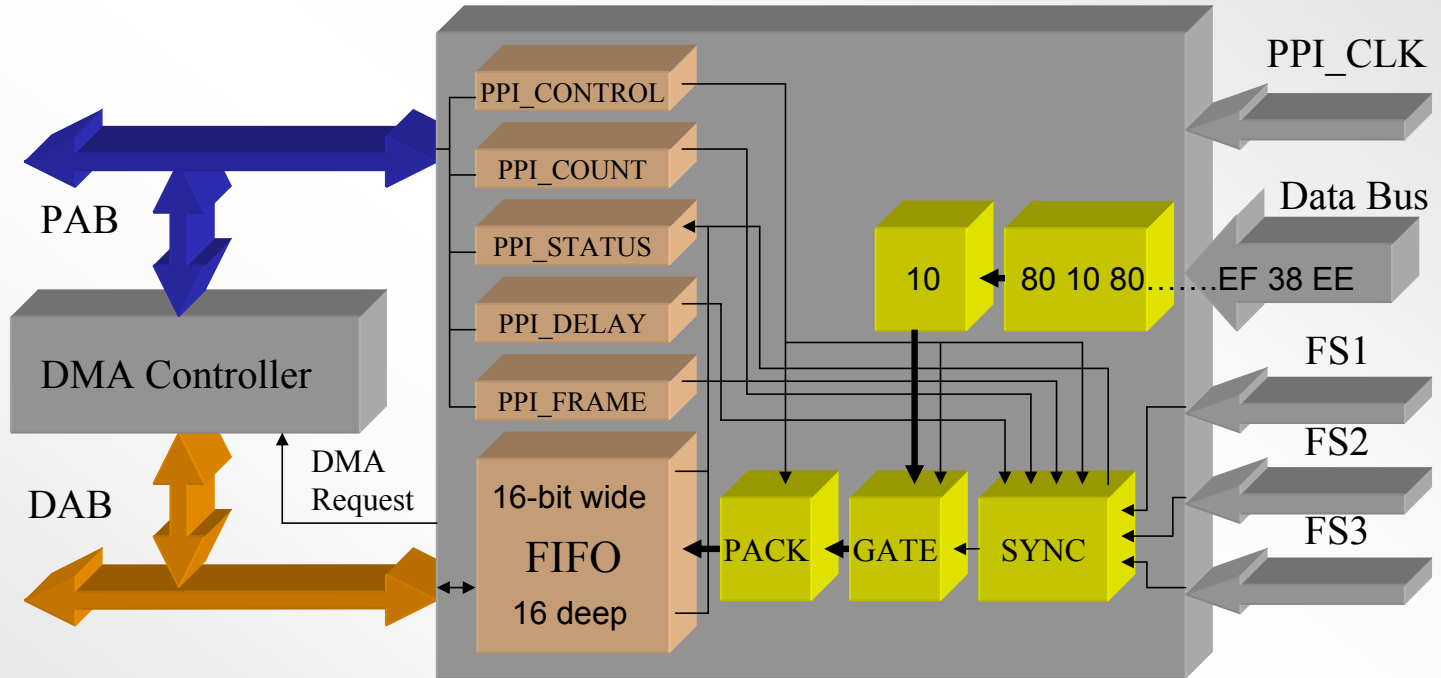
PPI in general purpose mode (For video and other high speed devices)



General Purpose Input/Output Modes

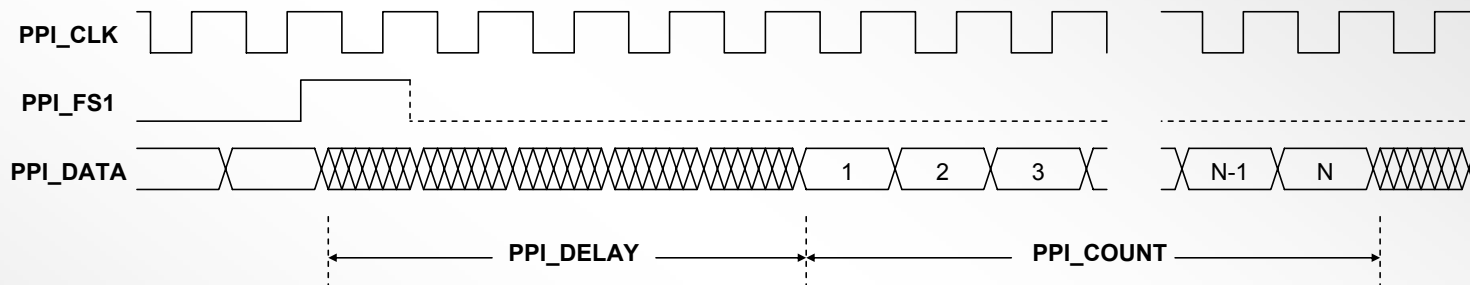
- **Single Sync (FS1 only)**
 - Useful for Data Converter applications
 - “Infinite Capture” input sub-mode requires either
 - initial H/W sync to be sent, or
 - “Self Trigger” through S/W write (no need for H/W FS)
- **3 Syncs (FS1, FS2, FS3)**
 - useful for video I/O with H/W signaling
 - “Frame Capture” mode outputs syncs from processor while data is input into processor
 - 2 Syncs can be used by ignoring 3rd sync where appropriate (pull FS3 to ground)
- **Modes are set in PPI_CONTROL register**

PPI General Purpose Input Mode



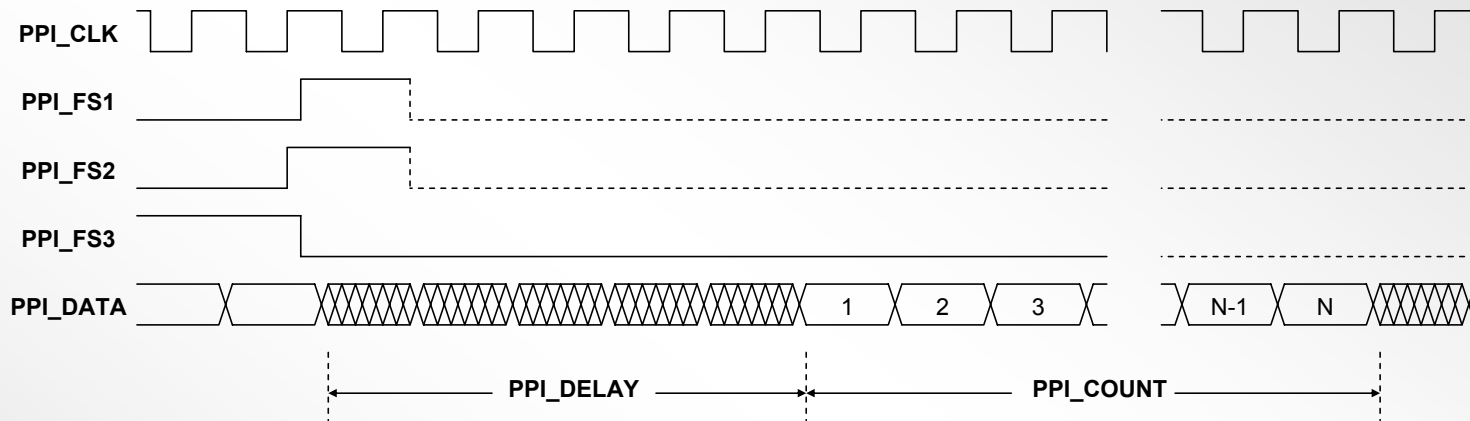
- PACK: 8->16-Bit Packing Unit
- GATE: Data Control Unit
- SYNC: Data Sync Unit

Single Sync Input Mode



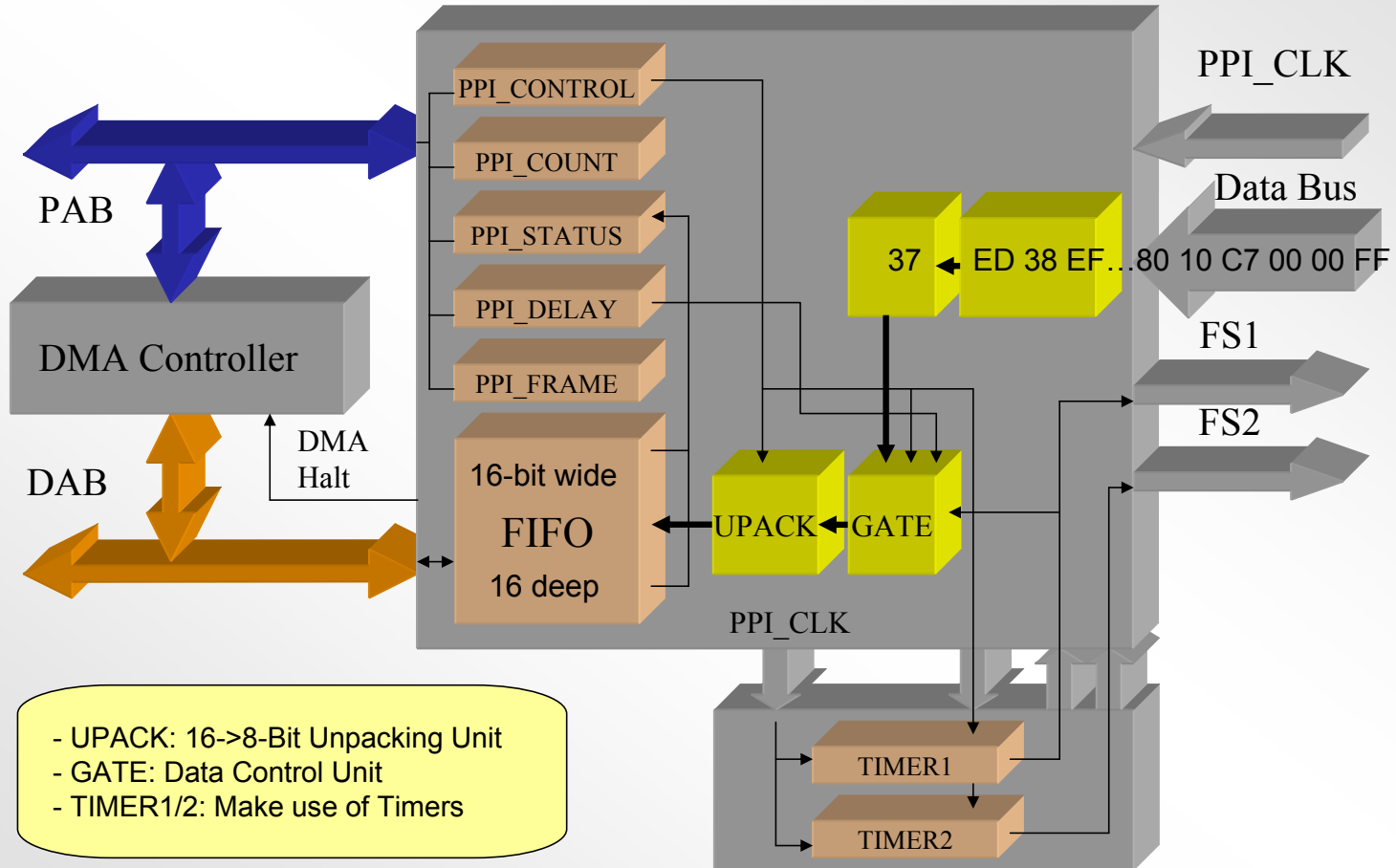
- PPI_CLK, PPI_FS1, PPI_DATA are inputs
- Programmable delay register (PPI_DELAY) inserts a time delay (in units of PPI_CLK cycles) to start transfer after FS1 has been asserted
- Count register (PPI_COUNT) holds the number of samples the PPI will receive
- PPI_COUNT ignored during Infinite Capture

Three Sync Input Mode

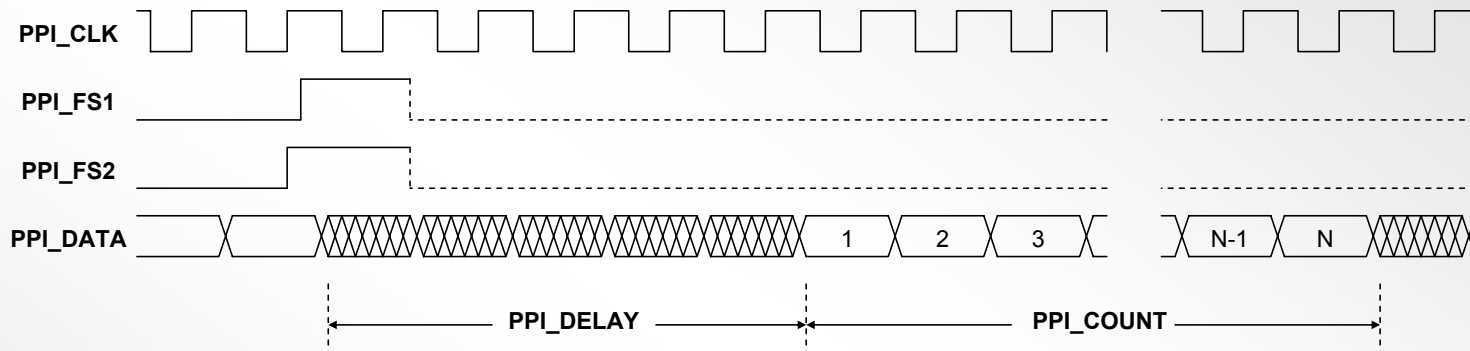


- **PPI_CLK, PPI_FS1/2/3, PPI_DATA** are inputs
- **Coincident assertion of FS1 and FS2 with FS3 low indicates the start of a frame**
 - FS3 used to indicate odd/even fields. In a 2-FSx configuration, this line is pulled low.
- **PPI_FRAME** register is set to the number of lines per frame (lines are delineated by FS1 assertions)

PPI General Purpose Input Mode Frame Capture

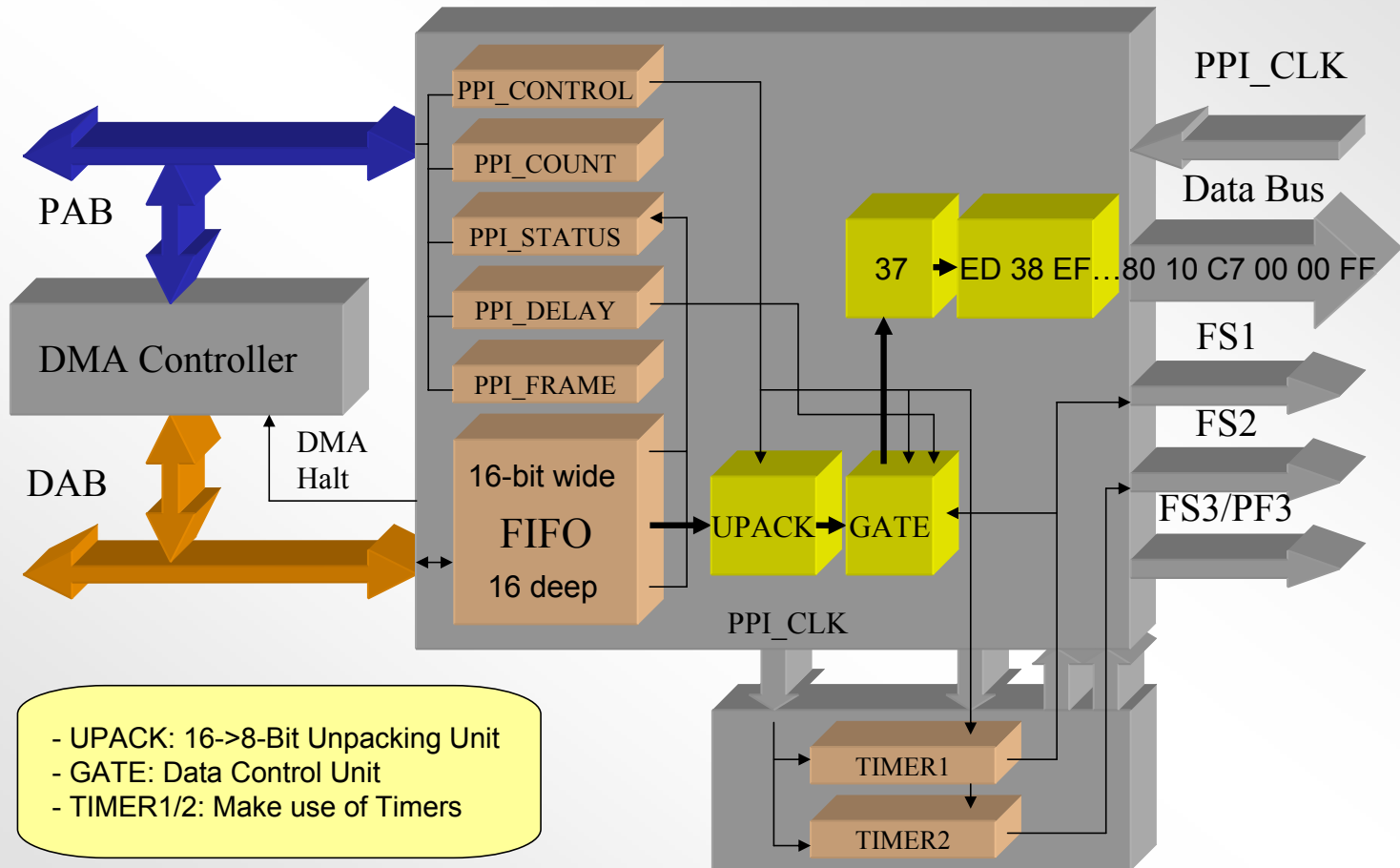


Frame Capture Input Mode



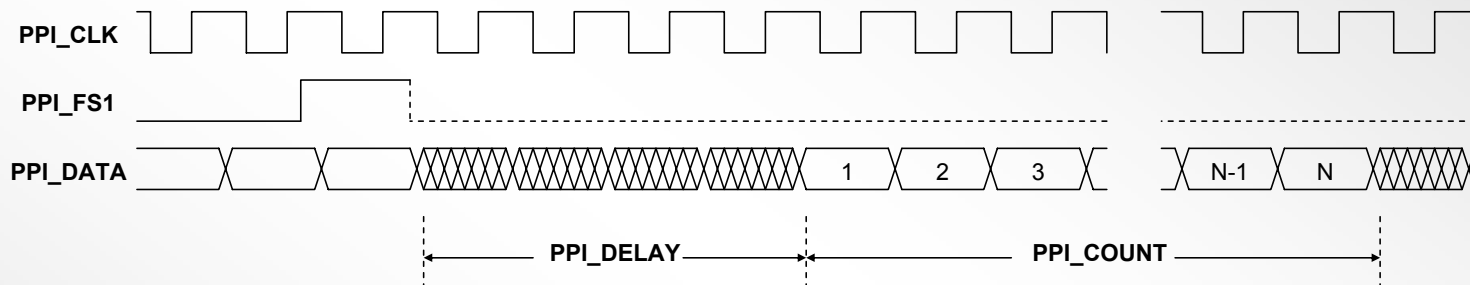
- **PPI_CLK, PPI_DATA** are inputs
- **PPI_FS1, PPI_FS2** are outputs
 - **TIMER1_WIDTH/TIMER1_PERIOD** used to set up **PPI_FS1** timing
 - **TIMER 2** set up to generate **PPI_FS2** timing
- **PPI_FRAME** register is set to the number of lines per frame (lines are delineated by **FS1** assertions)

PPI General Purpose Output Mode



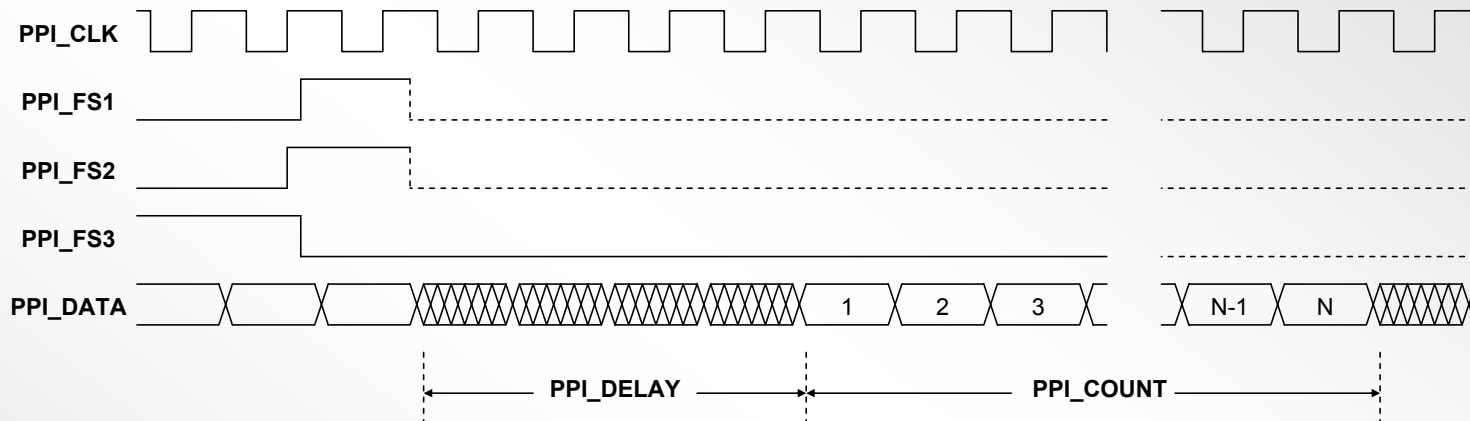
- UPACK: 16->8-Bit Unpacking Unit
- GATE: Data Control Unit
- TIMER1/2: Make use of Timers

Single Sync Output Mode



- PPI_CLK is input
- PPI_FS1 and PPI_DATA are outputs
 - Timer 1 used to set up timing for FS1
- There is a 1-cycle delay between FS1 assertion and start of PPI_DELAY
- Count register (PPI_COUNT) holds the number of samples the PPI will output, less one (i.e., set for N-1)

Three Sync Output Mode



- **PPI_CLK** is input
- **PPI_FS1, PPI_FS2, PPI_FS3** and **PPI_DATA** are outputs
 - Timer 1 used to set up timing for FS1
 - Timer 2 used to set up timing for FS2
 - FS3 toggles coincident with an FS1 assertion, after an FS2 assertion

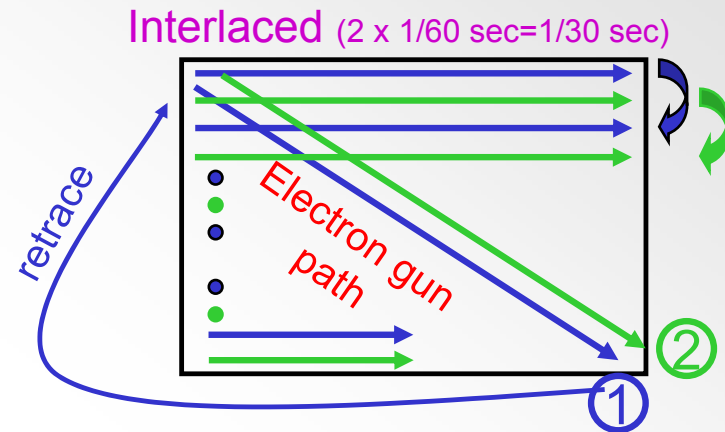
Video Basics

- **Screen Sizes**

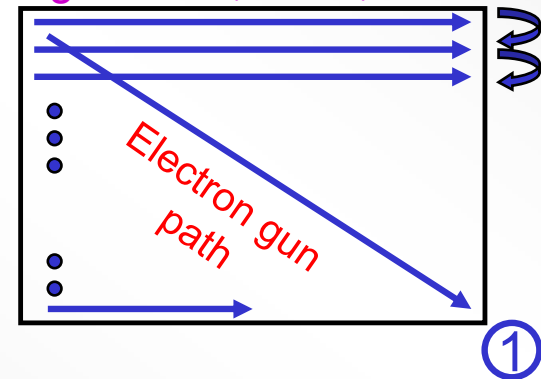
- QCIF = 176 x 144 pixels
- CIF = 352 x 288 pixels
- ¼ VGA = 320 x 240 pixels
- VGA = 640 x 480 pixels
- D1 (NTSC/PAL full screen)
= 720 x 480 pixels
[720 x 576 includes the unviewable portions above and below the picture]

- **Scan Types**

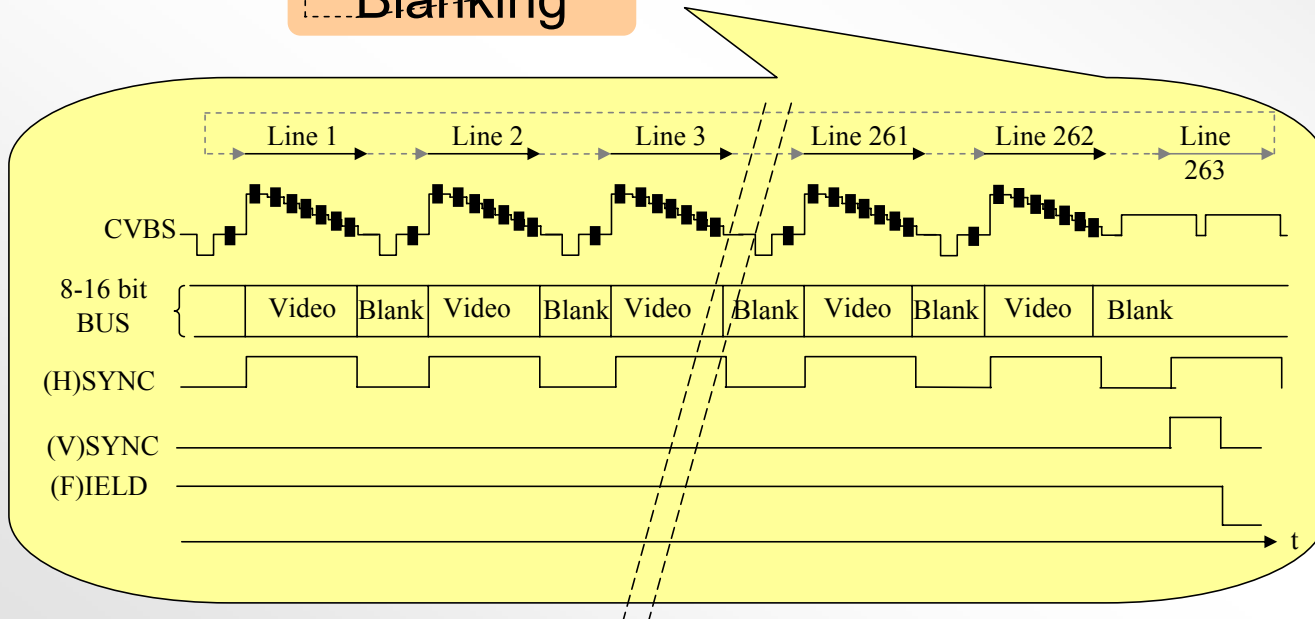
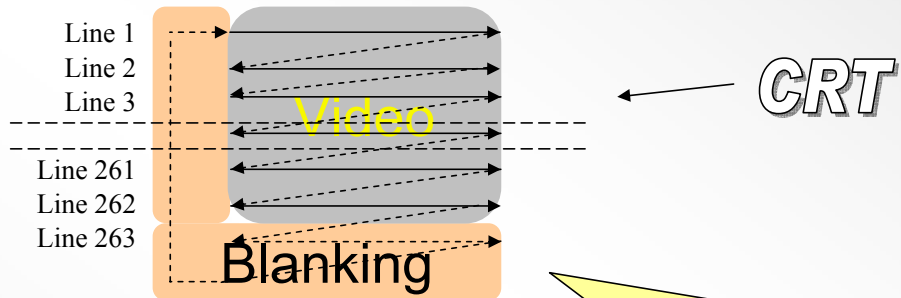
- Interlaced – dual-refresh technique on alternating lines at 1/60 second rate each (e.g. 1080i = 1080 horizontal lines interlaced)
- Progressive (Non-Interlaced) – single refresh technique on all lines at a 1/30 second rate (e.g. 480p = 480 horizontal lines progressive scan)



Progressive (1/30 sec)



Video Framing



What constitutes a 'pixel?'

- **Black-and-white image**
 - Y (luminance) values only; One 8- or 10-bit Y value per pixel
- **Color image**
 - RGB: Three 8- or 10-bit values per pixel
 - YUV: Scaled and decorrelated version of RGB
 - Y Cr Cb
 - One Y (luminance) value per pixel (720 per line)
 - One Cr or Cb (chrominance) value per pixel (360 of each per line)
 - 4:2:2 → 4 Y's for every 2 Cr's and 2 Cb's
 - Cb Y Cr Y Cb Y Cr Y Cb Y Cr Y Cb Y Cr Y

ITU-601

- **ITU-601 - specifies methods for digitally coding signals**
- **Video coding**
 - RGB is an intuitive format, but channels are highly correlated
 - YCrCb (a scaled and offset version of YUV color space) is highly uncorrelated
 - Provides better compression characteristics
 - 8-bit or 10-bit quantization
 - NTSC and PAL each have 720 pixels per line
 - NTSC (30 frames/sec) has 525 lines (including blanking)
 - PAL (25 frames/sec) has 625 lines (including blanking)
- PPI supports ITU-601 through use of 3-frame-sync modes

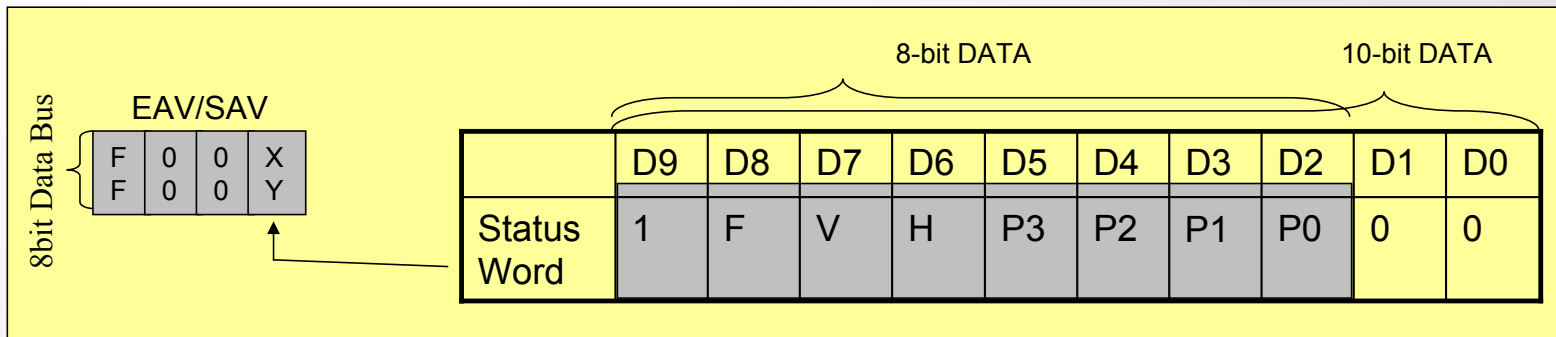
ITU-656

- **ITU-656**
 - **Defines the physical interfaces and data stream**
 - **Bit-parallel and bit-serial modes**
 - **Only bit-parallel supported with PPI**
 - **27 MHz nominal clock + 8-10 data lines (for bit-parallel mode)**
 - **Embedded hardware signaling (H, V, F) – no extra hardware lines required**
 - **Supports interlaced and progressive formats**
 - **Some OEMs support “pseudo” ITU-656**

PPI ITU-656 Modes

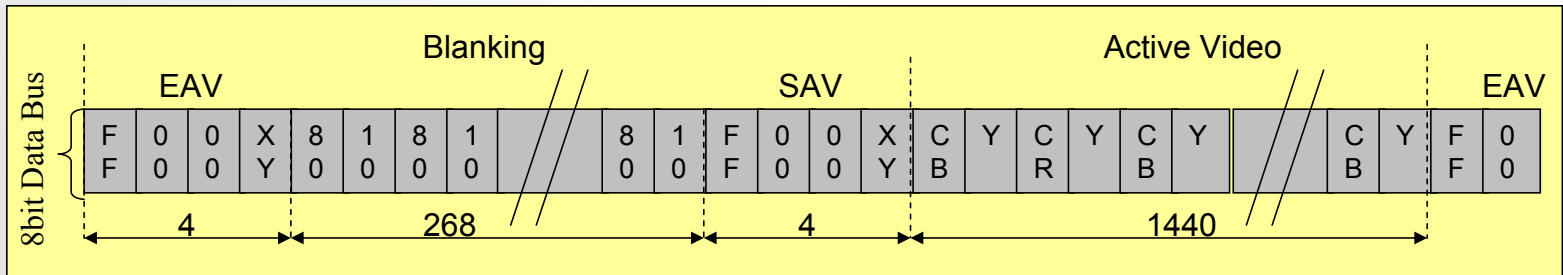
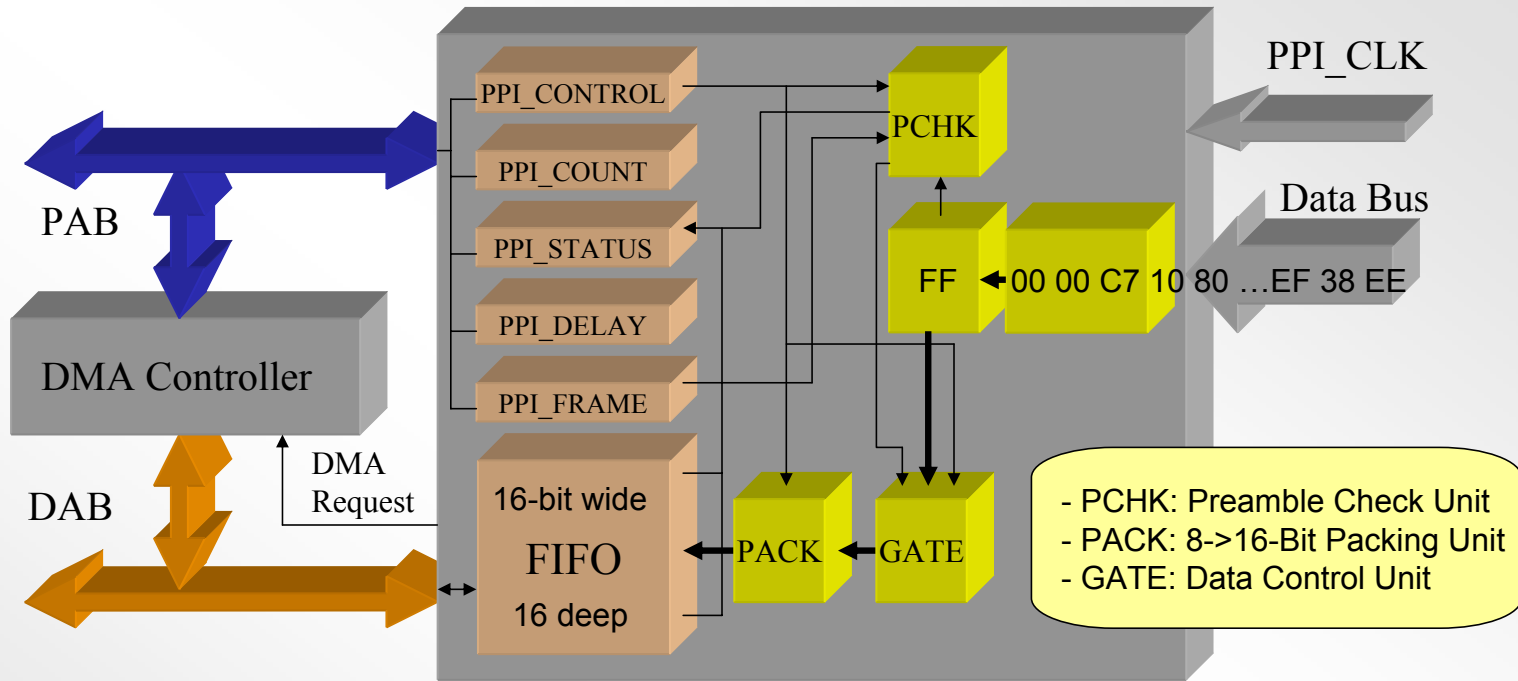
- **ITU-656 Input (3 Modes)**
 - Entire Field (H and V Blanking, Active Video and control codes)
 - Vertical Blanking Interval only (with associated H blanking and control codes)
 - Active video only. Can drop blanking for bandwidth savings
- **ITU-656 Output**
 - User sets up blanking and encoding info in memory

ITU-656 Mode Preamble

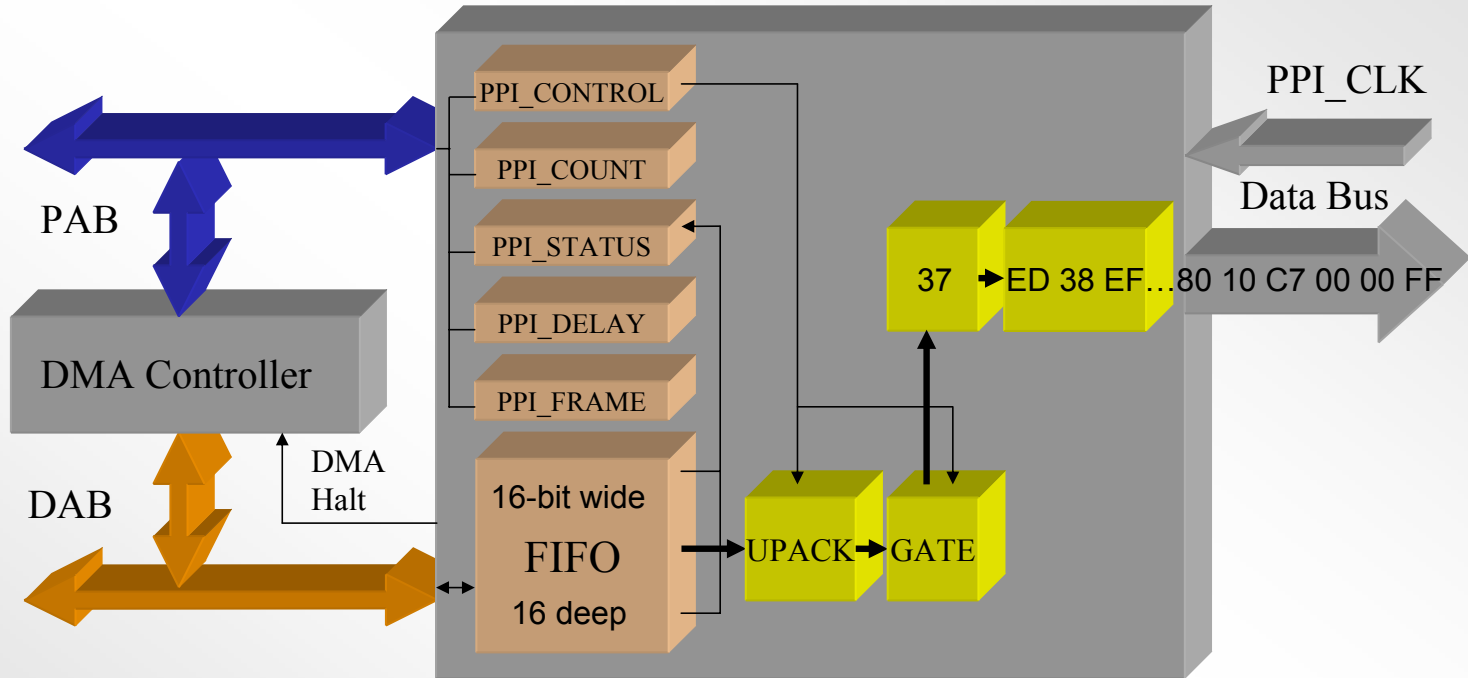


- The preamble (XY) holds the sync indicators “VSYNC, HSYNC, Field”.
- It also includes protection bits “P0-P3”.
- In output mode the user must construct all preamble control codes
- In general, the 8-bit bus is for consumer markets while 10-bit bus is for professional markets.

PPI ITU-656 Input Mode



PPI ITU-656 Output Mode



- UPACK: 16->8-Bit Unpacking Unit
- GATE: Data Control Unit

PPI Control Register (PPI_Control)

FLD_SEL (Active Field Select)

In ITU-656 input mode:

- 0 = Field 1
- 1 = Fields 1 and 2

In GP input mode:

- 0 = External frame sync trigger
- 1 = PPI self-trigger

PACK_EN (Packing Mode)

- 0 = Disable
- 1 = Enable

PORT_CFG[1:0] (Port Config.)

In input mode:

- 00 = 1 frame sync input
- 01 = frame capture, FS1, FS2 output
- 10 = 3 frame syncs
- 11 = infinite mode, 1 frame sync not repeated

In output mode:

- 00 = 1 sync
- 01 = 3 syncs

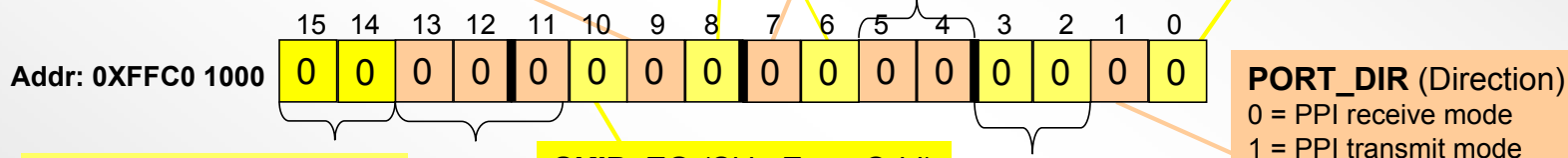
PORT_EN (Enable)

- 0 = PPI disable
- 1 = PPI enable

SKIP_EN (Skip Enable)

- 0 = Disable
- 1 = Enable

Reserved



PORT_DIR (Direction)

- 0 = PPI receive mode
- 1 = PPI transmit mode

POL[1:0] (Polarity)

00 = Nothing inverted

01 = PPI_CLK inv., PPI_FS1 and PPI_FS2 not inv.

10 = PPI_FS1 and PPI_FS2 inv., PPI_CLK not inverted

11 = PPI_FS1, PPI_FS2, and PPI_CLK inv.

SKIP_EO (Skip Even Odd)

- 0 = Skip odd number of elem.
- 1 = Skip even number of elem.

DLEN[2:0] (Data Length)

- 000 = 8-bit
- 001 = 10-bit

.

.

110 = 15-bit

111 = 16-bit

XFR_TYPE[1:0] (Transfer Type)

In input mode:

- 00 = Active field only
- 01 = Entire field
- 10 = Vertical Blanking only
- 11 = GP Input mode

In output mode:

- 00, 01, 10 = ITU-656 Output Mode
- 11 = GP Output Mode

PPI Status Register (PPI_STATUS)

ERR_NCOR (Error not corrected)

ITU-656 Mode:

0 = Preamble error detected and corrected
 1 = Preamble error detected but not corrected

OVR (PPI FIFO Overflow)

0 = No interrupt
 1 = FIFO Overflow Error interrupt occurred

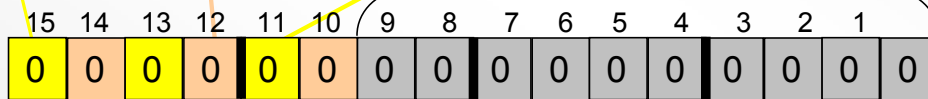
FT_ERR (Frame Track Error)

0 = No interrupt
 1 = Frame Track error interrupt occurred

Reserved

Read to clear

Addr: 0XFFC0 1004



ERR_DET (Error Detected)

ITU-656 Mode:

0 = No preamble error detected
 1 = Preamble error detected

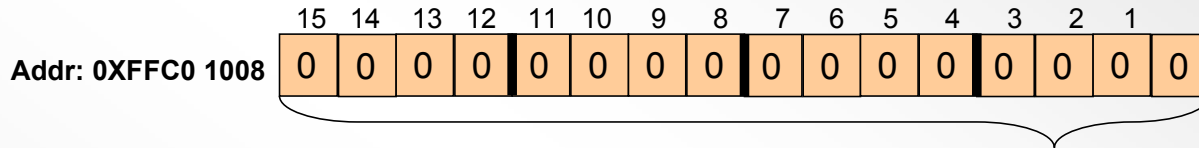
FLD (Field Indicator)

0 = Field 1
 1 = Field 2

UNDR (PPI FIFO Underrun)

0 = No interrupt
 1 = FIFO Underrun error interrupt occurred

Transfer Count Register (PPI_COUNT)



PPI_COUNT[15:0]

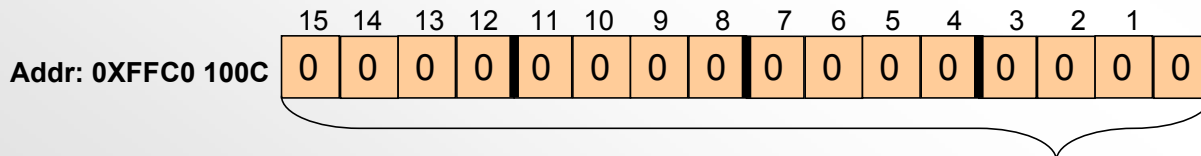
In GP input mode:

One less than the number of samples to read in to the PPI per line

In GP output mode:

One less than the number of samples to write out through the PPI per line

Delay Count Register (PPI_DELAY)

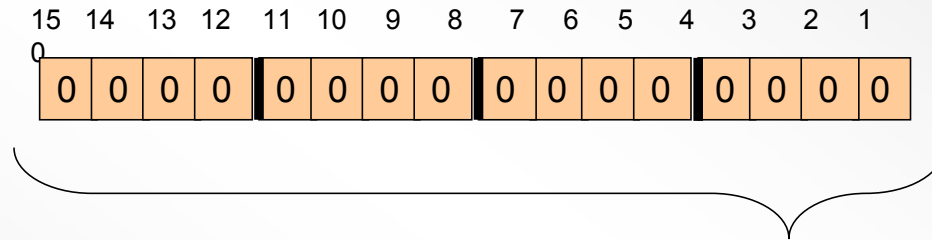


PPI_DELAY[15:0]

Number of PPI clock cycles to delay after assertion of PPI_FS1 before latching in data

Lines Per Frame Register (PPI_FRAME)

Addr: 0XFFC0 1000



PPI_FRAME[15:0]
Holds the number of lines
expected per frame of data